

**EXPERIMENTAL METHODS TO INFORM THERMAL
INTERFACE ENGINEERING IN HIGH POWER GAN DEVICES**

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
George W. Woodruff School of Mechanical Engineering

Georgia Institute of Technology
May 2019

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EXPERIMENTAL METHODS TO INFORM THERMAL INTERFACE ENGINEERING IN HIGH POWER GAN DEVICES

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To my family

ACKNOWLEDGEMENTS

I will begin this section as most others, by offering my most sincere thankfulness and gratitude to my PhD advisor, Professor Samuel Graham. It is difficult to convey the ways in which Dr. Graham's advisement and direction will have a lasting impact on my future. While he has always been more than helpful in providing scientific guidance through lengthy discussions, he has also played a critical role in demonstrating to me what a passionate, hardworking, and caring individual looks like. He conveys these traits not through his words, but through his actions. He is one of the most patient people I have ever met and has a way of motivating others, not by telling them to do something, but by taking the extra time to sit down and discuss many aspects of life, beyond just the research. It is obvious that he cares deeply for all the people in his life and strives every day to do what he can to ensure success in those around him. I will be forever grateful to Dr. Graham for his patience, understanding, trust, and encouragement throughout my PhD and beyond.

Countless individuals have contributed to my research and success here at Georgia Tech that it would take many pages to list each of them and the role they played. I will do my best to recognize those that have created a lasting impact on my experience at Tech, however, as I am sure to miss a few, please know that if you are reading this and I did not recognize you directly, it in no way diminishes the positive impact you have had on my life. I would first like to acknowledge and thank my PhD reading committee: Dr. Alan Doolittle, Dr. Satish Kumar, Dr. Asegun Henry, and Dr. Shannon Yee. Each of you have played an intricate role in contributing to my success through useful discussions, research collaborations, and relentless support in my abilities as a researcher. I would like to thank

Dr. Baratunde Cola for helpful discussions early on in my studies and for having confidence in me to use and learn his initial TDTR system. I would like to thank Professor Mark Goorsky and his graduate students for the wonderful TEM/SEM images and analysis they provided throughout this work.

I would like to Dr. Thomas Beechem for taking a chance on me as an undergraduate student at UNM. I was fortunate to be hired by him as a student intern at Sandia National Laboratories in 2012. His positive encouragement and overall excitement about research really resonated with me at the time. He taught me many valuable research lessons, not the least of which was effective communication and rigorous understanding of experimental uncertainties. He has continued to be a mentor and friend well beyond the length of my initial internship. I was fortunate to work with another terrific researcher early on at Tech, Dr. Thomas Bougher. He was extremely patient and helpful in working with me to learn all about TDTR. He was very thorough with data analysis and taught me the importance of correctly understanding and having confidence in data before reporting it. I thank him for the valuable experimental lessons he has taught me.

Contributions from several collaborators have ensured my success as a graduate student. I would like to thank IQE for providing useful samples. Specifically, Dr. Chien-Fong Lo and Dr. Hugues Marchand provided extremely help feedback and discussions. Qorvo provided several samples that were crucial to my research. Element Six and the Naval Research Laboratories have provided valuable diamond samples that have contributed greatly to this work. At Nagoya University I was able to work with Professor Hiroshi Amano. I would like to thank him for agreeing to host me for three months and the wonderful collaboration that has continued since that time. Dr. Kentaro Nagamatsu

provided valuable assistance in the epitaxial growth of the PN diodes evaluated in this work. I would like to thank Shigeyoshi Usami and Hayata Fukushima for performing the mesa etching and device fabrication of the GaN PN diodes and allowing me to watch and learn the process with them. I would also like to thank all the members of the Amano Lab, the secretaries, and Kat Mizutani for helping to make my experience in Japan extremely enjoyable.

I consider myself lucky to have worked with such a diverse and intelligent group of individuals in the Graham Group Lab. A special thanks to Dr. Georges Pavlidis. We began our PhD work at the same time and always had great discussions and enjoyed our time at multiple conferences together. Other members of the lab that were always available to provide help and expertise when needed include: Dr. Anne Mallow, Dr. Wale Odukomaiya, Dr. Ankit Kumar, Dr. Minseok Ha, Dr. Hyungchul Kim, Dr. Kyungjin Kim, Dr. Brian Foley, Dr. Darshan Pahinkar, Dr. Jingjing Shi, Nicholas Hines, Samuel Kim, Jason Jones, Yvette Chen, Kenechi Agbim, Kirkland Malcom, Waylon Puckett, Michael Sulkis, Gabe Cahn, Jason Hirschey, Brian Kelly, Priyanka Deo, and Robert Montgomery. A very special thanks to Zhe Cheng for always being available to discuss interesting problems and for motivating me to perform interesting research and write papers.

Outside of the Graham Group, many others contributed to my success. I would like to thank the students and friends that I worked with during the qualifying exams, Dr. Akanksha Menon, Dr. David Rodin, Alex Limia, and Eric Tervo. They were instrumental to me passing the exams. I would like to thank Dr. Kirash Gordiz for working with me to organize student thermal science seminars, as well as always having a positive attitude about life and research. Thank you to Dr. David Brown for useful discussions and insight.

I would like to thank Dr. Matthew Smith for his collaboration on interesting and unique entrepreneurial solar energy projects outside of my normal research. Dr. Manik Rajora, who was my roommate for almost five years in Atlanta, thank you for also being a great friend and constantly urging me to try new restaurants in Atlanta.

Finally, I would especially like to thank my family. Without their constant love, encouragement, and support I never could have made it this far. I would like to thank my older brother, Levi, for being a positive role model throughout my life and for taking the time to proof read some of my early documents and applications. Thank you to my parents, Bruce and Kelly, for always reminding me of the importance of education and for instilling excellent values in me that will last a lifetime. I cannot adequately express in writing the ways in which your love and support have shaped my life in such a positive way and have led to the accomplishment of my goals.

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LIST OF SYMBOLS AND ABBREVIATIONS

ABBREVIATIONS AND CHEMICAL FORMULAS

2-DEG	Two-dimensional electron gas
AC	Alternating current
AFM	Atomic force microscopy
Al	Aluminum
AlGaAs	Aluminum Gallium Arsenide
AlGaIn	Aluminum Gallium Indium Nitride
AlN	Aluminum Nitride
AMM	Acoustic mismatch model
Au	Gold
BFOM	Baliga's figure of merit
BiBO	Bismuth borate
C	Carbon
CCD	Charge-coupled device
CH ₄	Methane
CL	Cathodoluminescence
Cl ₂	Chlorine
Cp ₂ Mg	Bis(cyclopentadienyl)magnesium
CTE	Coefficient of thermal expansion
CVD	Chemical vapor deposition
DARPA	Defense Advanced Research Projects Agency
DC	Direct current

DMM	Diffuses mismatch model
DOS	Density of states
EBSD	Electron backscatter diffraction
EELS	Electron energy loss spectroscopy
EL	Electroluminescence
EOM	Electro-optic modulator
EPC	Efficient Power Conversion
FDTR	Frequency-domain thermorefectance
FEM	Finite element model
FET	Field-effect transistor
FIB	Focused ion beam milling
FWHM	Full width at half max
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GT	Georgia Institute of Technology
H	Hydrogen
HEMT	High electron mobility transistor
HFET	Heterojunction field-effect transistor
HEV	Hybrid electric vehicles
HPNS	High-pressure nitrogen solution
HP	High-power
HVPE	Hydride vapor phase epitaxy
ICMA	Interface conductance modal analysis
ICP	Inductively coupled plasma

IV	Current-Voltage
JFET	Junction gate field-effect transistor
LED	Light-emitting diode
LO	Longitudinal optical
LTi	Linear time invariant
MBE	Molecular beam epitaxy
MD	Molecular dynamics
MFP	Mean free path
Mg	Magnesium
MOCVD	Metal organic chemical vapor deposition
MOSFET	Metal oxide field effect transistor
NH ₃	Ammonia
Ni	Nickel
NJTT	Near Junction Thermal Transport
O ₂	Oxygen
PCD	Polycrystalline diamond
PL	Photoluminescence
RF	Radio frequency
RLC	Resistor-Inductor-Capacitor
SEM	Scanning electron microscopy
Si	Silicon
SiC	Silicon Carbide
SiN	Silicon Nitride
SL	Superlattice
STEM	Scanning transmission electron microscopy

TDD	Threading dislocation density
TDTR	Time-domain thermoreflectance
Ti	Titanium
TLM	Transfer length method
TMGa	Trimethylgallium
TTI	Transient thermoreflectance imaging
UID	Unintentionally doped
WBG	Wide band-gap
XRD	X-ray diffraction

SYMBOLS

A	Amplitude [μV]
a	Lattice constant [m]
α	Thermal penetration depth [m]
C_m	Thermal time constant weight parameter
c_p	Specific heat capacity [J/kg·K]
C_{th}	Coefficient of thermal reflectance [$^{\circ}\text{C}^{-1}$]
C_v	Volumetric heat capacity [J/m ³ K]
χ	Hankel transform variable
$D(\omega)$	Phonon density of states [s/rad·m ³]
ΔT	Temperature difference (T_2-T_1) [$^{\circ}\text{C}$]
E_F	Fermi energy [eV]
f	Frequency [Hz]

$f(\omega)$	Bose-Einstein distribution
$\Gamma_{1\rightarrow 2}$	Phonon transmission coefficient at interface
\hbar	Reduced Planck constant [eV·s]
h_{film}	Film thickness [nm]
h_K	Kapitza interface conductance [W/m ² K]
i	Imaginary number
j	Phonon branch indices
K	Spring constant [N/m]
k	Phonon wave vector [cm ⁻¹]
κ	Thermal conductivity [W/m-K]
k_D	Debye cutoff wave vector [cm ⁻¹]
λ	Wavelength [nm]
m	Mass [kg]
φ	Phase [rad]
Q	Pulse Energy [W]
q''	Heat flux [W/m ² K]
R	TDTR Ratio (-V _{in} /V _{out})
R_λ	Wavelength dependent reflectance
r	Radial coordinate [m]
ρ	Density [kg/m ³]
T	Temperature [°C]
T_∞	Steady-state temperature rise [°C]
t	Time [s]
τ_{echo}	Time [ps]

τ_m	Thermal time constant [μs]
TBC	Thermal boundary conductance [$\text{MW}/\text{m}^2\text{K}$]
TBR	Thermal boundary resistance [$\text{m}^2\text{K}/\text{GW}$]
Θ	Temperature in Hankel domain
θ	Angle [rad]
v	Acoustic sound velocity [m/s]
v_D	Debye group velocity [m/s]
v_g	Phonon group velocity [m/s]
V_{in}	In-phase TDTR signal [μV]
V_{out}	Out-of-phase TDTR signal [μV]
ω	Angular frequency [rad/s]
Z	Transfer function
z	Cross-plane coordinate [m]
z_A	Acoustic impedance [$\text{kg}/\text{m}^2\cdot\text{s}$]

SUMMARY

The development of high-power GaN HEMTs has created a significant opportunity for thermal engineers to better understand and manipulate nanoscale heat transfer mechanisms to aid in the thermal management of these devices. This is because current limitations in high-power GaN technologies exist due to thermal resistances in the device structures which impact heat dissipation during operation. The localized joule heating in the HEMT device concentrates an extremely large heat flux in thin device layers in the transistor channel. While much effort has gone into growing higher quality material to aid in both electronic and thermal properties, there is still significant research needed into understanding the role of thermal interface resistances inherent in these devices. Many times, the thermal boundary resistance (TBR) between the GaN and substrate can be a limiting factor in heat transfer away from the initial generation. Depending on the application, different substrates can be used during HEMT fabrication. Power devices are often grown on silicon substrates in order to take advantage of large area wafers and reduce cost. High-power RF devices however attempt to place high thermal conductivity substrates (such as diamond) close to the heat generation to remove heat as quickly as possible. In order to thoroughly investigate the impact interfacial layers have in these devices, experimental methods are used to evaluate the TBR for a series of GaN-on-Si wafers with varying interlayers. A complete analysis of material strain, TBR, and finally thermal device impact is presented. To examine the effectiveness of using a high thermally conductive material as a device substrate and heat spreader a series of bulk CVD diamond samples are evaluated along with thin films that range from 1 to 13.9 μm in thickness. An

in depth study of the impact of the dielectric layer on the TBR for a GaN on diamond device is carried out with CVD diamond that is grown on GaN using either an AlN or SiN interlayer and the TBR is evaluated as compared to a material system with no interlayer. Finally, a study of thermal transport in vertical GaN-on-GaN PN diodes was undertaken by evaluating the impact of polyimide passivation on device characteristics and heating. Followed by measurements of the thermal properties of the GaN due to doping effects with TDTR and full field transient thermal imaging of the device as compared to a thermal and FEM model to provide insight into thermal time constants and proper duty cycle operation.

CHAPTER 1. INTRODUCTION

1.1 Background and Motivation

The exponential increase in energy usage worldwide, the main source of which comes from fossil fuels that have been shown to cause irreparable damage to the environment [1], has created several social, economic, and scientific concerns. Our initial problem of converting and transmitting energy has been exacerbated into a much more difficult problem. How do we now do this in a way that keeps up with the demands of a growing population, causes the least amount of environmental damage, and provides consistent energy with little to no service interruptions? The solution to all of the aforementioned concerns may be advanced through the use of renewable resources, more efficient electronic devices, and implementation of smart grid technologies. While there are many factors that go into implementing each of the proposed solutions, one consistency among them is that pure silicon (Si) based power electronics will not be enough due to their inherent limitations defined by the material itself [2].

The implementation of next generation power grids capable of efficiently and effectively handling distributed generation from localized sources as well as several key technologies necessary to reduce the damaging effects on the environment will require power electronics that can handle higher voltages, operate at higher temperatures, and switch at faster speeds in a smaller form factor and do so more efficiently. Wide band-gap (WBG) power electronics based on gallium nitride (GaN) have the potential to fulfill the higher performance requirements for many of the previously mentioned applications. This is because, as a material, GaN exhibits properties superior to Si when considering high

voltage operation in a smaller form factor, high temperature stability, and high frequency operation. Figure 1 compares the relevant material properties that are attractive for semiconducting devices used in both power electronic and RF applications.

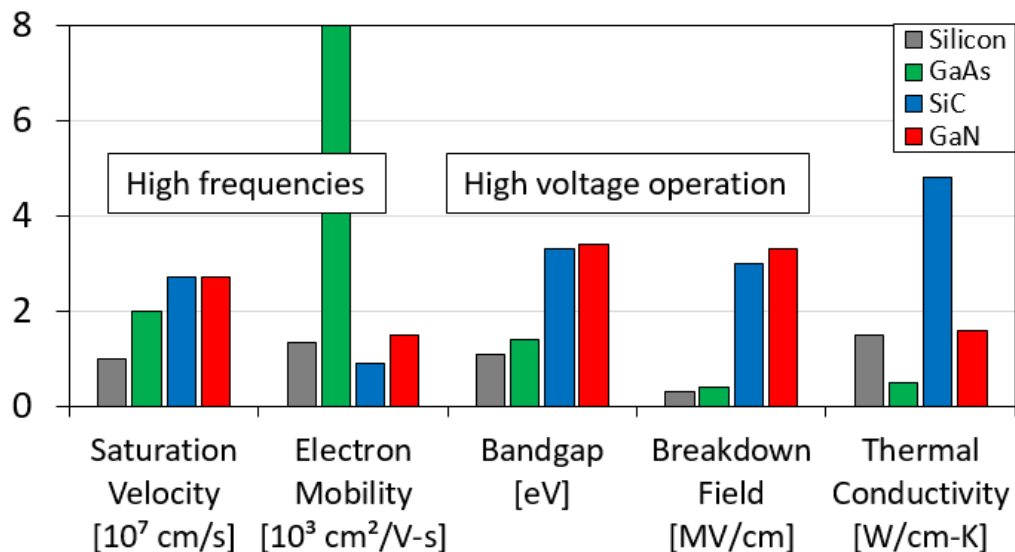


Figure 1. Comparison of materials properties relevant to semiconductors used to fabricate transistor and diode devices. GaN exhibits properties attractive to both power electronics and RF applications.

GaN has been used widely as a source material for blue light emitting diodes (LEDs) since the successful growth of high quality GaN on sapphire in 1986 and successful p-doping in order to create a PN junction LED in 1989 by Professor Hiroshi Amano [3, 4]. Since these achievements, research into the potential for GaN in a variety of optoelectronic applications has increased significantly [5-7]. More recently however, GaN has garnered attention for its potential to create more efficient power electronics and RF devices [8-14]. This is because high electron mobility transistors (HEMTs) based on GaN have been shown to demonstrate higher breakdown voltages, higher power densities, and a lower on-

resistance compared to both gallium arsenide (GaAs) based devices and state of the art Si devices [15, 16].

More recently, GaN has garnered attention for its potential to create more efficient power electronics. Power electronics are able to change the characteristics of voltage, current, and frequency in order to produce a desired output, for example switching from AC to DC or increasing/decreasing voltage. These devices are so ubiquitous in today's societies, that almost anyone living in an industrialized nation uses them multiple times every day without even realizing it [17]. At its core, this power switching ability is realized through the use of many electrical components, but transistors and diodes play a significant role in reducing the size and weight of the device, while also limiting the power handling capabilities [18]. Transistors and diodes also play a dominant role in dictating the efficiency of power transmission through the switching speed of the transistor, the reverse leakage current and the 'on-state' resistance of the device [19]. Because of the pervasiveness of power electronics, it is crucial for GaN technologies to reach a much lower price point in order to be competitive with Si and SiC based technologies. It is for this reason that much of the GaN power electronic applications are being manufactured on Si wafers using lateral HEMT devices [20]. Additionally, because of the significant maturity of Si wafer manufacturing many of the foundries have moved well beyond 8-inch wafer manufacturing thereby leaving this equipment underutilized [21]. It is desirable to take advantage of this and use the large area Si wafers as a substrate for GaN devices.

While much effort has been directed at the use of GaN in HEMTs, it is only recently that the prospect of vertical GaN PN diodes through the development of bulk GaN substrates has become possible [22, 23]. GaN PN diodes have demonstrated the potential

to succeed silicon-based devices in power applications based on their low on resistance and high breakdown voltages [24, 25]. Significant effort has gone into understanding and improving the electrical performance of GaN PN diodes, however, thermal characterization is lacking [26]. For high power applications it is especially important to understand how the underlying material characteristics inherent with the growth and development of the device structure affect the thermal performance and overall reliability of GaN devices.

1.2 GaN Devices

Electronic devices based on GaN have been demonstrated in both lateral and vertical architectures. With lateral devices typically fabricated as HEMTs [14], these devices have also been identified in literature as heterojunction field-effect transistors (HFETs) [27, 28]. For the purposes of this thesis, these lateral heterojunction devices with henceforth be referred to as HEMTs. The fundamentals and physics of an AlGaIn/GaN HEMT device will be explored in detail in Section 1.2.1. More recently, GaN has been incorporated in vertical device architectures [22, 23]. These consist of vertical transistors and diode structures. Both of which will be explained in further detail in Section 1.2.2. Finally, the many applications of GaN devices will be explained in further detail in Section 1.2.3.

1.2.1 AlGaIn/GaN High Electron Mobility Transistor

The idea of a heterojunction transistor was first realized by Mimura *et al.* [29] in 1980. In this early work, they accomplished the formation of a two-dimensional electron gas (2-DEG) through the use of n-type aluminum gallium arsenide (AlGaAs) doped with Si grown atop an undoped GaAs layer. Because of the higher electron affinity of GaAs, excess electrons from the doped AlGaAs are transferred into the lower bandgap GaAs

material. The free electrons gather in a potential well that is formed at the interface. This results in a very high carrier concentration in a very narrow region [30].

Similar to the AlGaAs/GaAs HEMT, the AlGaN/GaN HEMT also takes advantage of the creation of a 2-DEG. However, in the case of the AlGaN/GaN device, the 2-DEG can be created without additional doping required. This is because of the high levels of piezoelectric and spontaneous polarization that the materials exhibit. Spontaneous polarization is reference to the built-in potential difference in the crystal that is created simply by the preferential orientation of the atoms in the crystal. Because the bond between atoms is not purely covalent, the displacement of the electron cloud towards a particular atom is in the direction along which the crystal lacks inversion symmetry. This results in a net positive charge at a particular face of the crystal with a negative charge at the opposite face. In the case of the wurtzite phase of GaN this results in a strong polarization along the c-plane or [0001] direction with a negative charge on the Ga-face and a positive charge on the N-face. In addition to the spontaneous polarization, piezoelectric polarization plays a significant role in the formation of the 2-DEG. Piezoelectric polarization occurs when materials exhibit an electric field due to the distortion of the crystal lattice. AlGaN has a smaller in-plane lattice constant than that of GaN and decreases in size with the amount of the Al mole fraction, consistent with Vegard's Law [31]. The combination of spontaneous and piezoelectric polarization determines the net charge at an interface. AlGaN has a significantly larger spontaneous polarization than that of GaN and because the AlGaN is pseudomorphically grown onto the GaN as a thin layer, its lattice must undergo tensile strain in order to match the thick GaN with a larger lattice constant. This induces additional polarization at the AlGaN/GaN interface resulting in a net positive charge at the interface.

The positive sheet charge results in a layer that can be larger than 10^{13} cm^{-2} [32]. In the case of AlGa_N epitaxially grown on Ga_N the electric field generated can be on the order of 10^6 V/cm [33]. This is enough potential energy to cause loosely bonded electrons to ionize and drift towards the interface. These electrons move from the AlGa_N into the Ga_N. However, because of the large bandgap differences in the materials, a 2-DEG is formed when the electrons fall into the quantum well. The 2-DEG sheet charge density is therefore typically around 10^{13} cm^{-2} , which is significantly larger than that of an AlGaAs/GaAs based 2-DEG [34]. A schematic of the polarization charges can be seen in Figure 2.

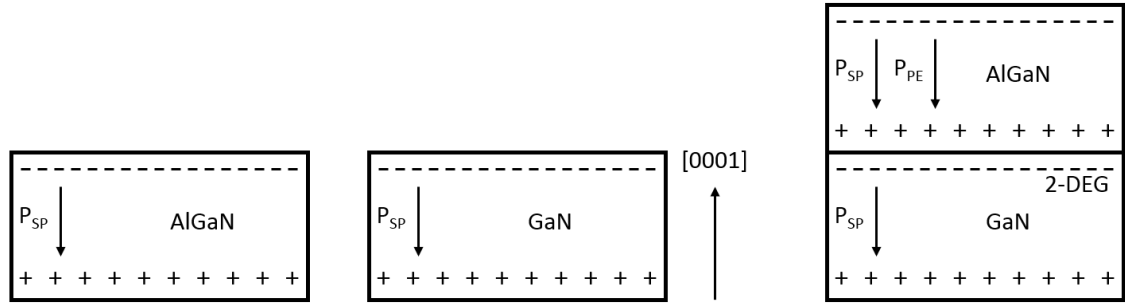


Figure 2. Sheet charges due to spontaneous polarization in AlGa_N and Ga_N along with piezoelectric polarization in the AlGa_N help to create a positive polarization at the AlGa_N/Ga_N interface when materials are pseudomorphically grown. This along with the large bandgap difference leads to the formation of a 2-DEG in the Ga_N at the interface. Adapted from [30]

It is interesting to compare the impact of both the polarization components on the conduction band edge of the AlGa_N/Ga_N heterostructure. Figure 3 shows the impact each of the components have on inducing the formation of a 2-DEG. The 2-DEG is formed when the interface of the conduction band edge dips sharply below the Fermi energy (E_F). Without polarization effects considered no 2-DEG is formed, while when neglecting only

the spontaneous polarization component it is still possible to form a 2-DEG only accounting for piezoelectric induced polarization.

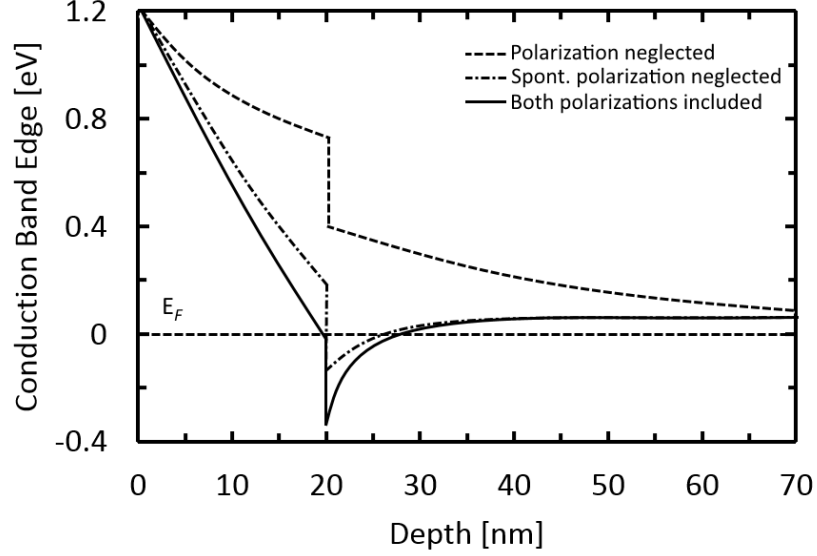


Figure 3. Conduction band edge for an AlGaIn/GaN heterojunction demonstrating the impact of polarization charges on the formation of the 2-DEG. Adapted from [35].

Fabrication of GaN HEMTs are normally achieved through the epitaxial growth of the GaN on top of a suitable substrate. Typically, the substrate material consists of SiC, sapphire, or Si, however more recent work has looked at development of GaN HEMTs on less traditional substrates such as diamond, bulk GaN, and AlN [36-40]. In all substrate cases except for the bulk GaN a buffer layer is typically used in order to facilitate the growth of high quality GaN that is suitable for device fabrication. The quality of the GaN is typically quantified by looking at number of threading dislocations [41, 42]. Depending on the growth method and substrate/buffer layers used the threading dislocation density (TDD) has been shown to range from 10^9 cm^{-2} to 10^6 cm^{-2} , with few dislocations present when GaN is grown on top of a native GaN substrate with no buffer layer.

A traditional AlGaIn/GaN HEMT structure is shown in Figure 4. It is clear from the figure that the current flows laterally in the ohmic contacts from the drain to the source. Unlike traditional enhancement mode metal oxide semiconductor field effect transistors (MOSFET) most HEMT devices are constructed as “normally-on” devices. This means that a negative bias between the gate and source is required in order to keep current from flowing between the drain and source. In the scenario that a GaN HEMT is used in a power supply circuit that fails, a “normally-on” device would allow current to continue to flow and cause a potentially dangerous situation. There are however fabrication and circuit design techniques that allow for “normally-off” operation in GaN HEMTs, albeit with some performance trade-offs [43-45].

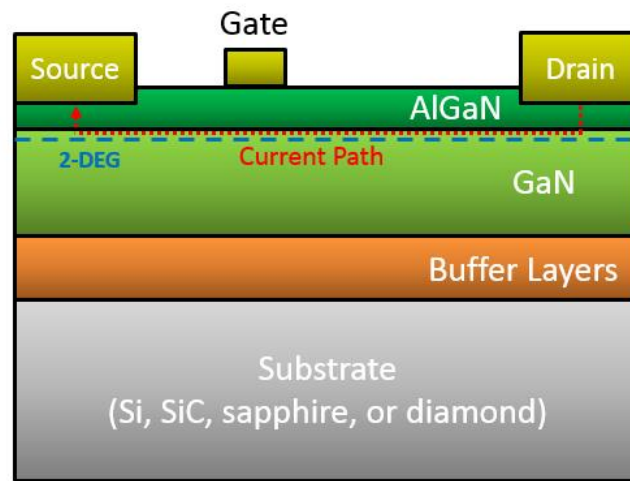


Figure 4. Simple AlGaIn/GaN HEMT device demonstrating lateral current flow from the drain to source contact.

The unique design and physics of AlGaIn/GaN HEMTs allow for their potential use in a variety of applications ranging from microwave RF systems to high power electronic conversion systems. The many applications of GaN devices will be discussed in subsection

1.2.3 However, there are still significant reliability issues that arise due to both structural and thermal issues. Section 1.3 will describe each of these concerns in more detail.

1.2.2 Vertical Devices

One important metric that is considered when designing solid state transistors and diodes is that of breakdown voltage. This metric is considered in Figure 1 by looking at the breakdown field of the material itself. GaN has a breakdown field of about 3.3 MV/cm, which is a little more than 10 times larger than that of Si (0.3 MV/cm) [46]. Effectively this means that for the same voltage requirements a GaN device could be made with about 10x less material than Si. However, one significant difference is that Si technology is much more advanced and can be grown using the Czochralski process. This process has been shown to produce large quantities of very high-quality mono-crystalline material [47]. This allows for Si devices to be very easily fabricated in a vertical fashion. Leaving much of the surface area for device fabrication. In the case of AlGaIn/GaN HEMTs the most effective way of creating high voltage power devices is to increase the distance between the source and drain. Additionally, for high voltage operation, the electric field also extends vertically through the GaN thickness. Because of the heteroepitaxial growth of the GaN during fabrication, the GaN thickness is typically limited to less than 15 μm based on a variety of factors such as substrate choice, growth method, and wafer size [48-50]. The thickness limitation comes from stress incurred during the growth process that has been shown to cause cracking of the GaN substrate at critical thicknesses [51, 52]. The impact of strain in thin layers of GaN, specifically for the case of GaN-on-Si, will be discussed in more detail in Section 4. In this case it is difficult to take full advantage of the larger breakdown field in GaN simply due to growth and manufacturing constraints. It is for these reasons that

the development of vertical GaN devices is crucial to continue the advancement and applicability of wide-bandgap electronic devices.

Vertical devices can be fabricated on bulk GaN substrates as well as non-native substrates. However, with the later devices they are typically referred to as quasi-vertical and are severely limited due to the previously discussed GaN thickness limitations. It is only recently that high quality bulk GaN wafers are becoming available commercially [53]. Bulk GaN is grown using one of four methods: hydride vapor phase epitaxy (HVPE), ammonothermal method, high-pressure nitrogen solution growth (HPNS), or Na-flux method [54]. In contrast to Si, which has high-quality low-cost substrates, the GaN-based device technology is more advanced than its bulk crystal growth technology. Each of the aforementioned methods have their own unique advantages and disadvantages such as complexity/cost, growth rate, and dislocation densities, however one of the common factors among them is that the lateral substrate size is still limited to less than 6" in diameter [54].

When discussing vertical devices, it is important to consider the many types of vertical transistors and diodes. At the heart of most semiconducting devices lies the PN junction. While details of pn junctions have been exhaustively covered in both textbooks and literature [55, 56], the idea will be briefly described here. In a semiconductor device select regions are doped with either acceptor (p-type) or donor (n-type) atoms that cause those regions in the material to have either an excess or a deficiency of electrons. Where carriers in the p-type and n-type region are referred to as holes and electrons respectively. When these two regions in a material exists in intimate contact a pn junction is formed. If the carrier concentrations are equivalent in the two regions, the junction is referred to as a

step junction. At the interface of this junction excess carriers of each type diffuse into the opposite regions creating what is typically referred to as a depletion region. This region essentially defines the amount of voltage that is required to allow current to flow through the material and is extremely important in device design. Depending on how the doping profiles exist in the material it is possible to design both a field effect transistor (FET) and a diode. In the FET, current flow is impacted by applying specific voltages to the gate contact, where-as in a diode, the device is designed to only allow current flow in one direction from the anode to the cathode. Figure 5 displays simple schematics of a common junction gate field-effect transistor (JFET) and a common pn diode structure both developed on bulk GaN substrates.

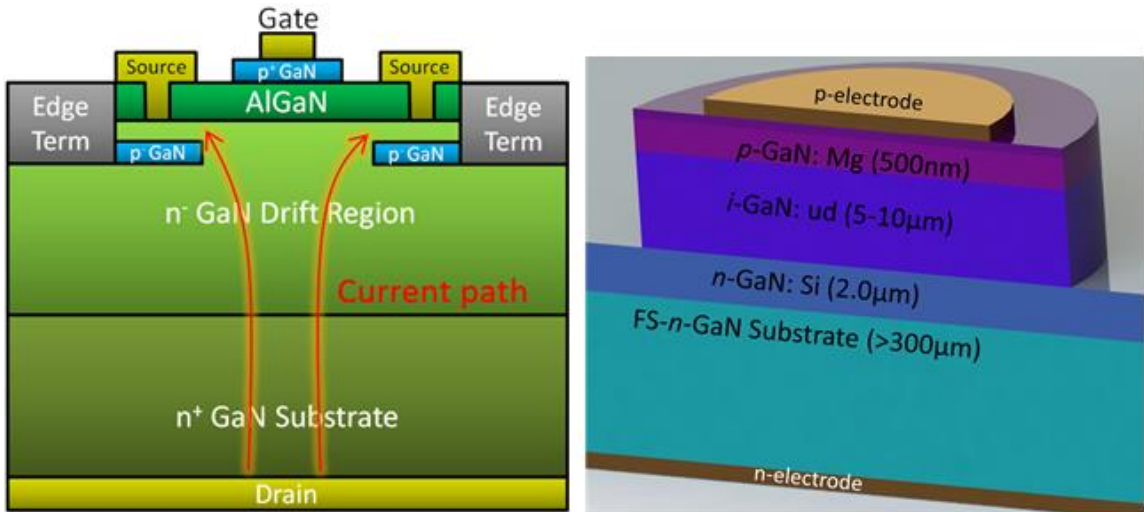


Figure 5. Typical vertical GaN devices. (Left) A JFET device demonstrating current flow from drain to source with select regions of p and n-type doping. Adapted from [53]. (Right) A traditional pn diode structure with anode (p-type) contact and cathode (n-type) contact. In this structure, current will flow from the anode to the cathode.

While there are several different types of iterations of the vertical transistor, the basic idea of selectively doping particular regions remains the most difficult challenge.

Lack of selective area doping, or regrowth processes limit the full potential of vertical GaN transistors. Current methods such as ion-implantation or select area diffusion of p-type dopants has not produced select regions with sufficient quality as compared to that of an equivalently grown pn junction [57]. The aforementioned difficulties of device fabrication along with the lack of maturity in bulk GaN substrates and high associated costs have led to a relatively slow adaption of bulk GaN devices, however, there is still much interest and research motivating the adaptation of said devices due to their potential benefit in power device applications.

1.2.3 Applications

Perhaps the most well-known application of a GaN device is that of the previously mentioned blue LED [4], however, there are numerous device applications beyond the DC operation found in LEDs. Specifically, GaN HEMTs have already seen commercial success from companies such as Transphorm, Wolfspeed, Qorvo, GaN Systems, Infineon, Panasonic, and Efficient Power Conversion Corporation (EPC). While these companies and more provide prepackaged GaN transistors, they are forced to place significant limitations on operating parameters such as switching speeds and operating voltages. This is mainly due to significant reliability concerns that are still being addressed regarding the mechanical and thermal aspects of HEMT device operation. There are currently no commercially available vertical GaN devices in the form of transistors or diodes [53] due to the previously mentioned cost and manufacturing/reliability issues.

Both vertical and lateral GaN devices have a plethora of potential applications. These applications are typically divided up into two categories. Either fast switching (RF

applications) or power switching. RF electronics typically operate at switching frequencies between 20kHz up to 300 GHz, with the majority being used for power amplification in wireless communication, satellite, and radar systems [58-60]. For RF applications lateral devices are typically desired due to the ability to design and manufacture the devices with very little distance between the gate, drain, and source contacts. By reducing the distance between contacts, the device can switch on/off at higher frequencies. However, a significant drawback to closely spaced contacts and fast switching is the materials ability to remove the large heat flux between switching events and the thermal crosstalk between the hot spots leads to large temperature differentials. While it is desirable to operate at both high frequencies and high-power densities for many applications, reliability issues stemming from the significant heating is currently limiting this potential.

In terms of power switching devices, both lateral and vertical GaN devices are required to fulfill the full spectrum of potential applications. Examples of a power electronic system consist of a solar inverter that would be used to convert 48 V DC power to 220 V AC power, an electric motor drive that uses 200 V DC power from a car battery to drive a 650 V AC motor, and finally a simple laptop charger that would convert 110 V AC from the electrical outlet to 19 V DC power [25]. Figure 6 demonstrates several potential GaN power device applications and their corresponding power ranges [61]. For applications that require relatively small voltage blocking (<600 V) lateral devices grown on Si offer many advantages to that of a bulk GaN device. The main advantage being cost but reliability due to the technology's maturity is also a significant factor. In the case of lateral power devices, it is possible to achieve higher breakdown voltages and capabilities by simply increasing the distance between the gate, drain, and source contacts. As

previously discussed, this however has its limitations due to limits on the GaN thickness during the growth process. In order to effectively utilize GaN in applications such as photovoltaic inverters, wind turbines, and motor drives, bulk GaN devices are desired. In the automotive industry there is a strong demand for GaN devices in regard to AC charging systems and DC/DC power conversion found in both electric and hybrid electric vehicles (HEV) [62]. As one might imagine, it is extremely important for vehicles to reduce the size and weight of their components in order to increase the efficiency of a limited fuel tank or battery. GaN technologies have the capability of significant size/weight reduction with increased power efficiency.

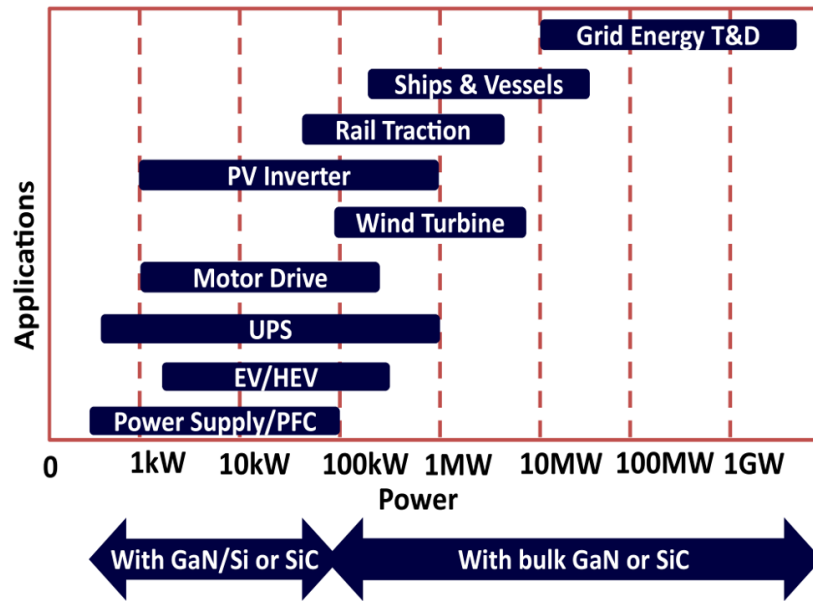


Figure 6. Power requirements for several potential GaN applications considering both lateral devices on non-native substrates and bulk GaN devices [61].

A buck converter is a circuit that is designed to perform a DC/DC power conversion by stepping down a high voltage DC source to a smaller voltage. This circuit consists of both a transistor and a diode, along with inductors, capacitors, and resistors. The basic

principle works by charging and discharging the capacitance side of the circuit such that the output voltage oscillates at a desired output. A simple schematic of a buck converter is shown in Figure 7 with the input and output characteristics. In this case the main power loss consists of limitations in the transistor and diodes. It is desirable to have as little loss as possible in order to both increase the device efficiency and reduce thermal impacts as the power loss is realized in the form of additional heat generation.

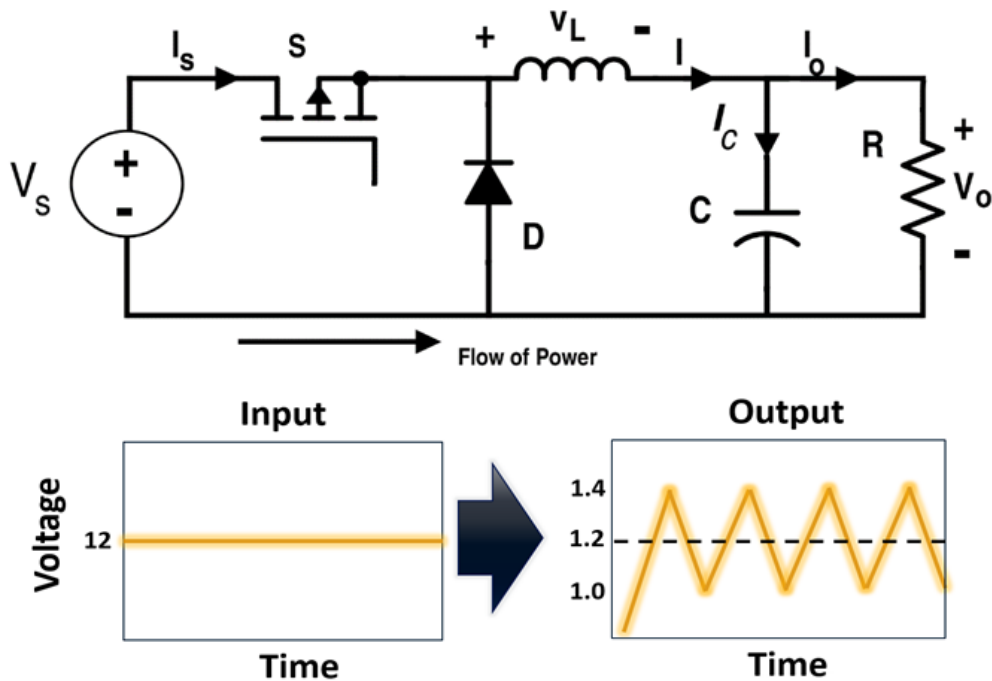


Figure 7. Simple buck converter circuit that could be used to convert 12 V DC power to 1.2 V DC power as might be used in a computer power supply.

The superior material properties of GaN compared to Si allow for much faster switching events. This can be seen in Figure 8 when comparing a similar GaN and Si device, the GaN is able to turn on approximately 10 times faster. This leads to reduced power loss during the switching event. Which also leads to a reduction in external electronic components such as inductors and capacitors in the circuit, thereby reducing the

size and weight of the overall module. Besides the power loss due to reverse leakage current, and the on-state resistance of both diodes and transistors, the switching event is where the most significant loss of power is realized, so by implementing devices that allow the power electronic circuit to switch at faster frequencies, the overall efficiency of the circuit is increased [63]. Figure 9 demonstrates the relationship between device switching and power loss.

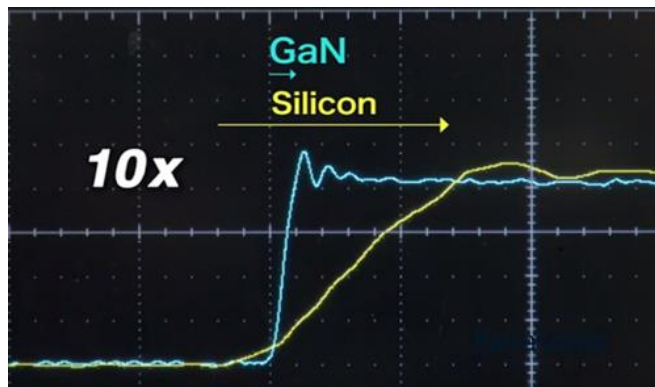


Figure 8. Demonstration of similar GaN and Silicon devices switching from an off to an on state [64].

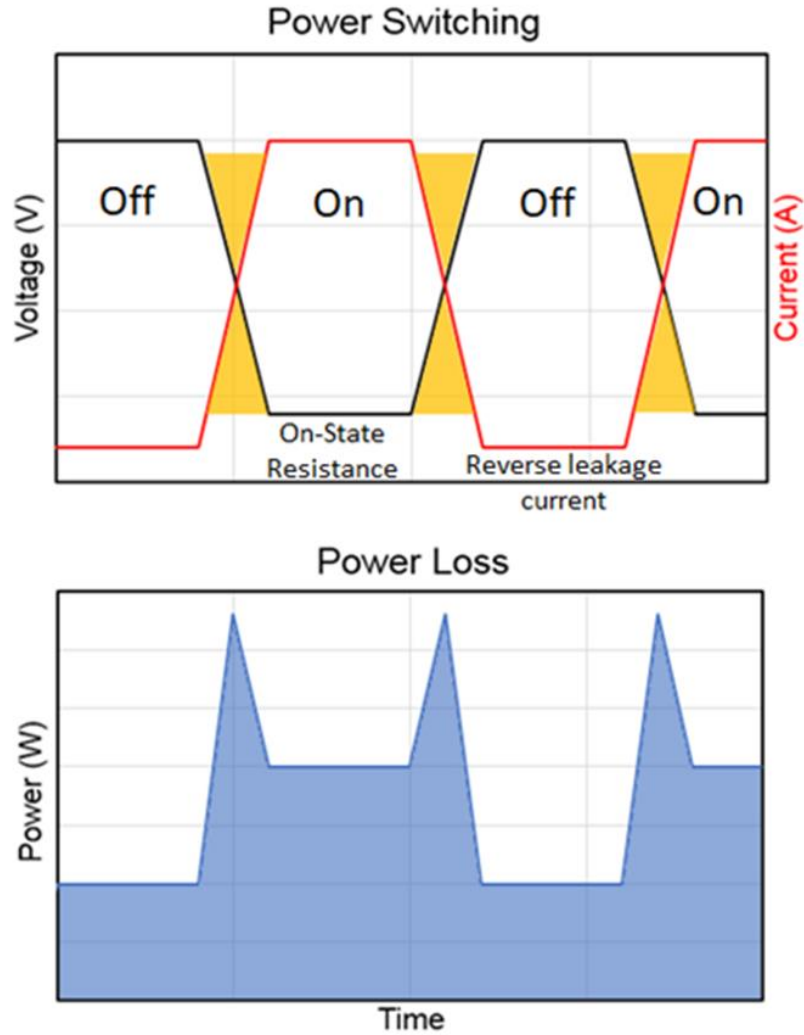


Figure 9. (Top) Voltage and current characteristics vs time of a generic power device during switching from its off to on state. (Bottom) Associated power loss during each state and switching event.

Understanding of loss mechanisms and thermal limitations is paramount to increasing the adaptation of GaN based devices. Reliability concerns that stem from both thermal and mechanical issues will be discussed in further detail in Section 1.3, with a specific look at the role that the thermal boundary resistance due to epitaxial growth and device fabrication has in limiting device performance, lifetime, and reliability being expounded upon in Section 1.4

1.3 GaN Device Reliability

As with any relatively new type of technology or electronic device, understanding and addressing the reliability and lifetime concerns are paramount to its adoption. Regarding GaN devices there are both significant mechanical concerns in the form of stress gradients that occur both from the epitaxial growth as well as during device operation and thermal concerns that are inherent in the operational device physics of a HEMT device. Specifically, in normally-on HEMT devices there is typically a large voltage bias between the source and drain and as the device is transitioning to an on-state there is still a negative bias between the source and gate. In this condition, a large acceleration of electrons is realized on the drain side of the gate causing a large electric field and the dissipation of thermal energy. The electrons dissipate their thermal energy in the form of longitudinal optical (LO) phonons, which will be discussed further in Section 2.1. In order to give up the energy to the crystal lattice and begin removal of the heat through diffusion, the LO phonons must decay into acoustic phonons in the material. Because this process is not instantaneous and the speed at which the electron energy is realized as joule heating is much faster than the removal of the heat by acoustic phonons, an extremely large heat flux become apparent on the drain side of the gate. Figure 10 demonstrates the large potential difference during device operation and the subsequent localized heating. This localized heating and large electric field has been shown to have deleterious effects on the device reliability and operation in the form of contact degradation [65] and hot electron induced trap generation [66].

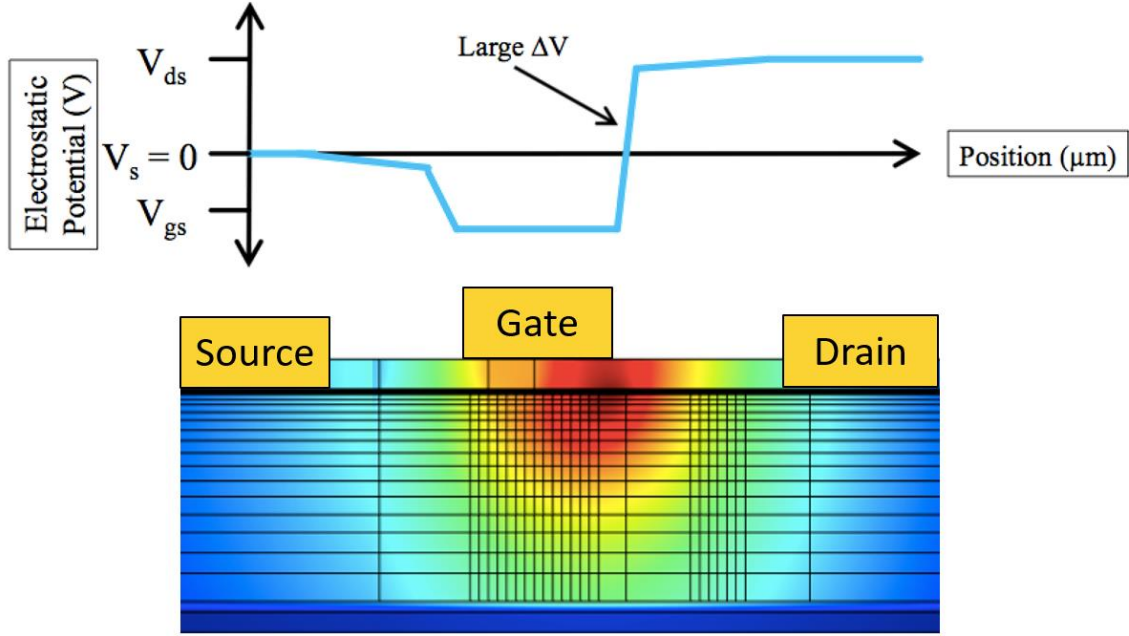


Figure 10. Demonstration of large potential gradient in a GaN HEMT device and subsequent localized heating on the drain side of the gate contact.

1.3.1 Stress Management

As mentioned, stress can play a significant role in the degradation and reduced performance/lifetime of a GaN device. Several degradation mechanisms have been outlined by previous researchers but there is still ongoing effort into fully understanding the contributions of each mechanism to the degradations of the device [67-69]. The sources of stress in the device material come from the residual stress induced during the epitaxial growth process, the thermal stress due to constrained thermal expansion during device operation, and the inverse piezoelectric stress (a direct consequence of the piezoelectric nature of the material that allows for the 2-DEG formation) that comes from the rapidly changing electric fields. Each of these stress issues has been addressed in different ways in the literature. Specifically, the piezoelectric stress impact has been mitigated to some extent

using a source or gate connected field plate [70]. The field plate essentially smooths the peak electric field and reduces the large gradient seen in Figure 10. This effect has been studied in detail previously [71].

Residual stress is realized in both the AlGaN and GaN material of a HEMT device. This is because the fabrication process requires epitaxial growth of the GaN on non-native substrates. The GaN and the substrate are not perfectly latticed matched and have different coefficients of thermal expansion (CTE). Because of this residual stress arises in the GaN layer during the high temperature growth process due to both to the forced lattice matching and differencing expansion and contraction rates as a function of the growth temperature. Depending on the substrate, it is possible to induce either compressive or tensile stress in the GaN material [72]. However, in all cases, the pseudomorphic growth of the AlGaN on top of the GaN layer will induce additional tensile stress in the AlGaN, which is crucial to effectively create the 2-DEG but can also lead to reliability issues when the additional piezoelectric and thermal stresses are present during device operation [71]. Mitigation of the residual stress is often achieved using additional growth layers between the substrate and the GaN. These additional interlayers depend on the substrate material and the design requirements. Specifically, GaN-on-Si stress management and device impacts will be discussed in detail in Section 4.2

Finally, thermal stress has been shown to contribute significantly to device degradation [71]. During device operation there is constant compressive thermal stress near the drain edge side of the gate. The large localized heat flux causes the material to want to expand, however it is constrained due to the surrounding cooler material. The large thermal gradient and CTE mismatch between the materials generate thermal stress, which

can be a contributing factor in premature device failure. Additionally, localized heating and stress can degrade performance by causing a reduction in electron mobility and drift velocity, because of increased carrier scattering. Mitigation of thermal stress is crucial to device performance and reliability and is typically achieved using substrates with high thermal conductivities such as SiC. More recently however, researchers have explored the use of heat spreading layers such as diamond on top of the device in order to reduce the heat flux by spreading out the effective heating area. Also, the use of diamond substrates has been of great interest in the development of high power GaN devices.

1.3.2 Thermal Management

Thermal management is key to increasing a devices performance and reliability. The exceedingly high-power densities at which GaN devices can operate ($> 30 \text{ W/mm}$) [33] have been estimated to roughly equivalent to that of the surface of the sun [73]. The significant self-heating in a GaN HEMT has a negative impact on thermal transport in the device due to many factors. The thermal conductivity of a material is a function of temperature and with increasing temperature a reduction in GaN thermal conductivity is realized due to enhanced phonon scattering. A more in-depth discussion of phonons and thermal conductivity will be explored in Section 2.1. In addition to the reduced thermal transport the mobility and drift velocity of electrons is also reduced due to the optical phonon scattering. This in turn has a negative impact on the device performance by decreasing the output current for an applied voltage and the operational frequency. The thermal impact on IV characteristics can be seen in Figure 11. When a device is operated under a DC condition the self-heating creates mobility issues as mentioned above and this in turn leads to a thermal droop or reduction in the output current. However, if the same

device is operated under a pulsed condition, the thermal droop is avoided, and the saturation current of the IV curve remains consistent.

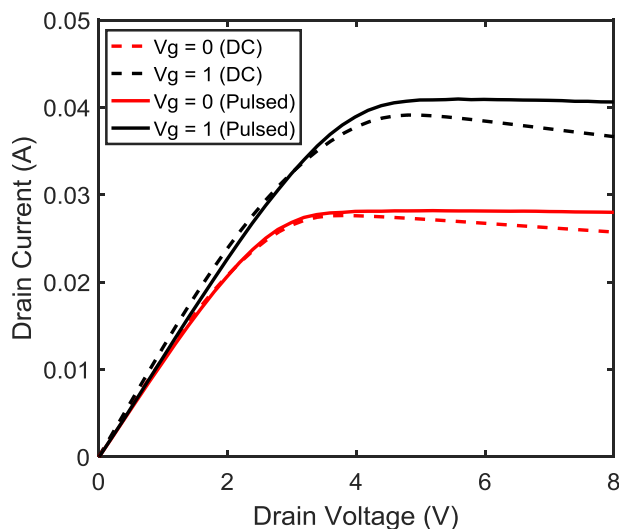


Figure 11. IV characteristics of a GaN on Si HEMT when operated under a DC and pulsed condition.

It has also been shown that self-heating and large heat fluxes in GaN HEMT devices can cause issues with the Schottky and ohmic contacts, causing degradation or even diffusion of the metal into the AlGaN material [70]. All these reliability issues combine to limit the performance and lifetime of the device. While each issue has been and is still currently being investigated [74], the relative impacts are often realized as an increase in operational temperature. Figure 12 shows the median lifetime of a GaN on SiC device as a function of channel temperature. Significant lifetime reduction is realized when a GaN HEMT device operates with a high channel temperature. For this reason and many others, it is imperative that the heat generated in the channel is removed from the device as quickly as possible.

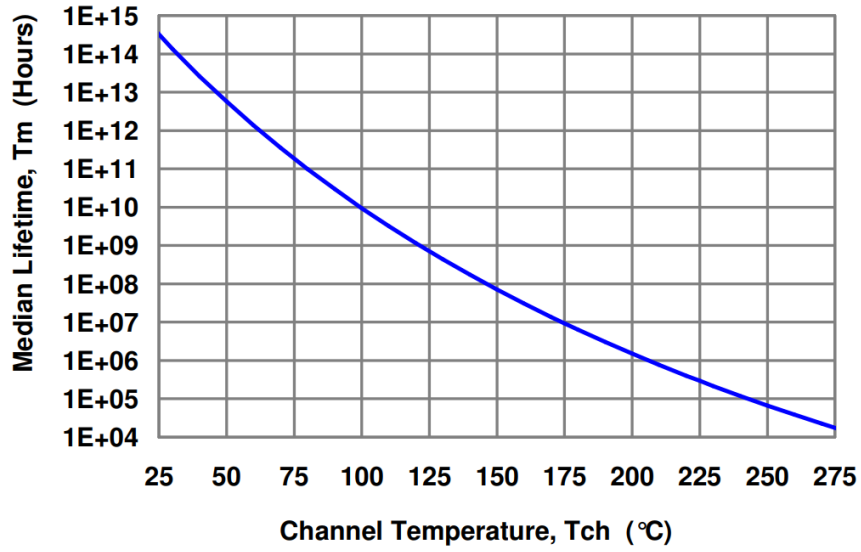


Figure 12. Median Lifetime of a GaN on SiC HEMT device as a function of channel temperature [75].

Mitigation of the intense heating found in the GaN HEMT has been addressed in several ways. Use of a field plate to spread out the electric field can cause a slight reduction in peak channel temperature [71], however the concern of the field plate is typically more attributed to piezoelectric effects rather than thermal. Recent studies have looked at the use of heat spreading layers of diamond and graphene/graphite [76, 77]. Others have examined the impact of etching away part of the substrate and refilling with a high thermal conductivity material such as AlN, diamond, or copper in order to create a thermal via to allow for heat transfer [78]. While one of the most obvious and well-studied approaches consists of simply using high thermally conductive substrates such as SiC or diamond. SiC is the preferred substrate for GaN HEMTs used in RF applications due to previously discussed spacing considerations, however, with significant advances in the growth of synthetic diamond, it is now being realistically considered as a potential GaN HEMT substrate material. Previous studies performed as a part of the Near Junction Thermal

Transport (NJTT) program through the Defense Advanced Research Projects Agency (DARPA) were able to achieve a 2.7x reduction in the thermal resistivity of a HEMT device as compared to a GaN-on-SiC device. They also demonstrated a 3x increase in the areal dissipation density of GaN-on-diamond compared to GaN-on-SiC [79]. Of course, diamond and SiC substrates can be relatively expensive when compared to Si. The thermal impact of GaN-on-Si devices will be explored in detail in Section 4 using multiple experimental methods. In regards to GaN-on-diamond, it was found in the previous study from Altman *et al.* that the relatively large TBR of $47.6 \text{ m}^2\text{K/GW}$ was a significant factor in limiting the device performance [79]. When considering both diamond and Si as device substrates the TBR can be a significant bottleneck for heat transfer and cause elevated temperatures in the device channels.

1.4 Thermal Boundary Resistance (TBR)

The interface between two different materials creates a thermal impedance. In other words, heat transfer across an interface is not continuous as it is in the material. Rather dissimilar materials create a very abrupt temperature difference over an atomically small distance. This leads to an increase in temperature between the heat source and the cold sink. The change in temperature at a given interface is often referred to as the thermal interface resistance and consists of two components. The thermal contact resistance and the thermal boundary resistance (TBR), both are expressed in units of $\text{m}^2\text{K/W}$, or the ratio of the temperature change for a given area over the total thermal power input. The contact resistance comes from the roughness between two materials. When materials are brought together, they are often not in intimate contact due to some surface roughness present on each material. The reduction of heat flow is primarily attributed to a reduction in contact

area of the solids due to surface roughness that allows a significant portion of the contact area to be filled with low thermal conductivity air (0.026 W/m-K). This is well defined for a macroscopic system and can be easily measured [80]. However, during epitaxial growth, the atoms at the surface often form an intimate bond with the adjacent material such that no air pockets exist. However, in this situation there still exists a TBR that is due to a difference in the vibrational properties or phonon density of states between the two materials. The idea of phonons and their dispersions will be discussed in detail in Section 2.1. As the TBR is reduced the maximum temperature in the heat source is reduced. Analogous to TBR is the thermal boundary conductance or TBC. When discussing heat transfer these terms are related as their inverse. In mathematical terms the TBC is defined as the proportionality constant related to the change in temperature across an interface for a given heat flux, $q'' = TBC(\Delta T)$ and has units of W/m²K. As mentioned earlier the TBR is simply the inverse of the TBC as, $TBR = 1/TBC$.

1.4.1 *Impact on Devices*

The impact of TBR on device performance and heating has already been lightly discussed. As mentioned, a large TBR between two materials translates directly into a higher operating temperature in a GaN device. Several theoretical predictions [81, 82] along with experimental efforts [83-85] have been made in order to better understand how the TBR between a GaN HEMT and substrate impacts the operational temperature in a device. The relationship between GaN/substrate TBR and the thermal conductivity of the substrate is of great significance. An illustrative example of how heat must flow through a lateral GaN device to the substrate is shown in Figure 13 along with an example of how different transition layers are accomplished through the use of either a SL structure or a

simple transition layer. These transition layers are necessary in order to allow for high quality GaN growth and combat structural issues that arise due to different material CTE's and the different lattice constants. Incorporation of transition layers help to grade out the lattice mismatch between the substrate and GaN.

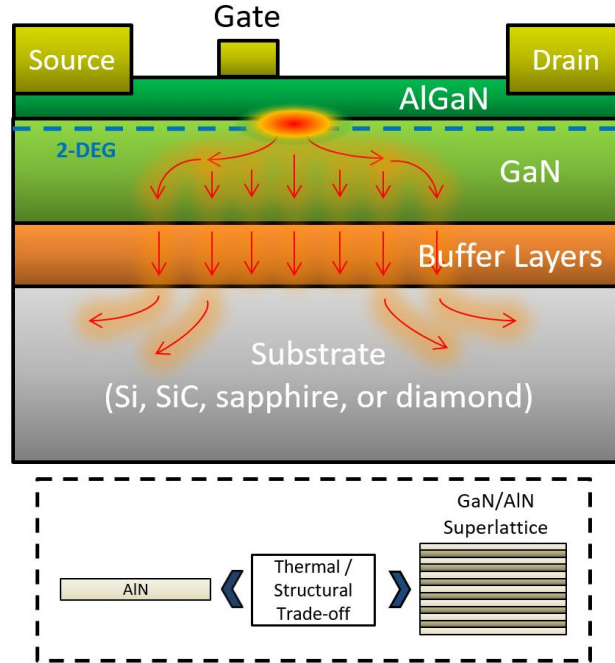


Figure 13. A traditional GaN HEMT device demonstrating the source of heat generation on the drain side of gate and the path through which the heat must flow. The buffer layers will typically consist of a simple transition consisting only of AlN/AlGaN or may contain much more complex SL layers that result in an increased thermal resistance between the GaN and substrate.

As an example, a GaN HEMT device was modeled using an analytical approach from Bagnall *et al.* [86]. The model consisted of a 3 μm GaN layer atop a substrate consisting of either high quality diamond, SiC, or Si. The GaN layer was prescribed an isotropic thermal conductivity of 160 W/m-K, while the substrate thermal conductivities were varied accordingly and are illustrated in Figure 14. A TBR between the GaN/substrate

of $10 \text{ m}^2\text{K/GW}$ was applied to the model. The modeled structure was a 10-finger device with $50 \text{ }\mu\text{m}$ gate-to-gate spacing. The heat sources were each assumed to be $4 \times 150 \text{ }\mu\text{m}$ and the total domain was $2000 \times 2000 \text{ }\mu\text{m}$. A total power density of 10 W/mm was applied to the simulated device. The device structure and the corresponding temperature distribution across the center of the fingers for each substrate is shown in Figure 14. From this model it is clear that the implementation of a high thermal conductivity substrate can significantly reduce the overall temperature rise in a device as well as mitigate the increased temperature between the gate fingers.

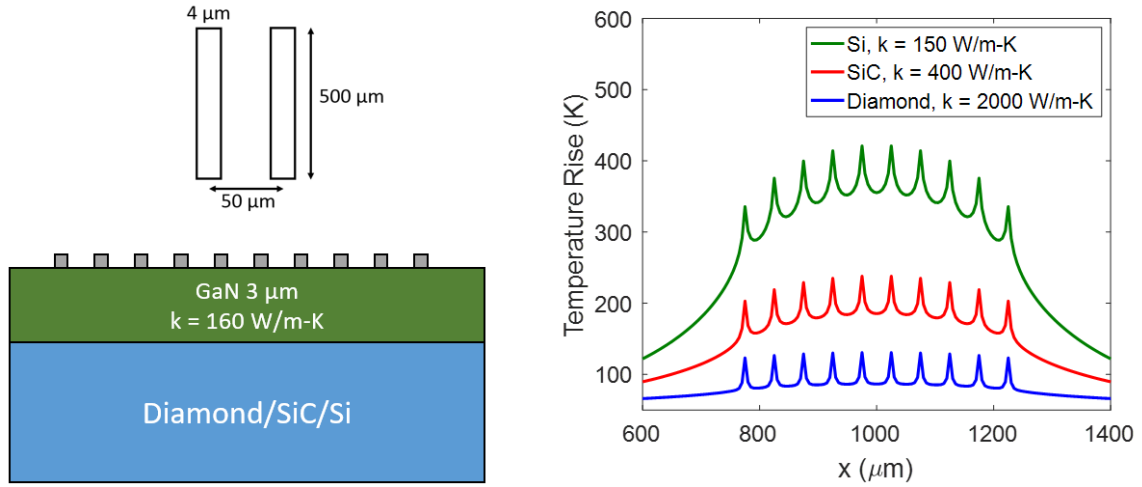


Figure 14. (Left) Schematic of modeled device. (Right) Heating profile across the center of the fingers demonstrating impact of different commonly used substrates.

While the substrate choice can have a significant impact on operational temperature and allow for devices of larger power densities, as has been discussed, issues of cost, manufacturing capabilities, and desired device application also play a significant role in the substrate choice. The impact of TBR for GaN-on-Si and GaN-on-diamond devices will be discussed in further detail in Chapters 4 and 5 respectively, so for comparative purposes the impact of TBR for a GaN-on-SiC device will be used here as an example of the impact

of TBR on operational device temperature. Several experimental techniques including Raman thermometry, TDTR, and transient interferometric mapping have been used to estimate the TBR for GaN-on-SiC. These values have been found to range from 4 to 120 $\text{m}^2\text{K}/\text{GW}$ dependent upon the growth methods and the transition/adhesion layers [83, 84, 87, 88]. Using the previously described model, the temperature profile through the depth of the material is plotted as a function of distance with varying TBR values as seen in Figure 15. An abrupt temperature difference is observed at the interface in all cases where a TBR is present and has a direct impact on the maximum temperature. An additional parametric study was done to observe the maximum junction temperature as a function of the TBR for a GaN-on-SiC device and can be seen in Figure 15.

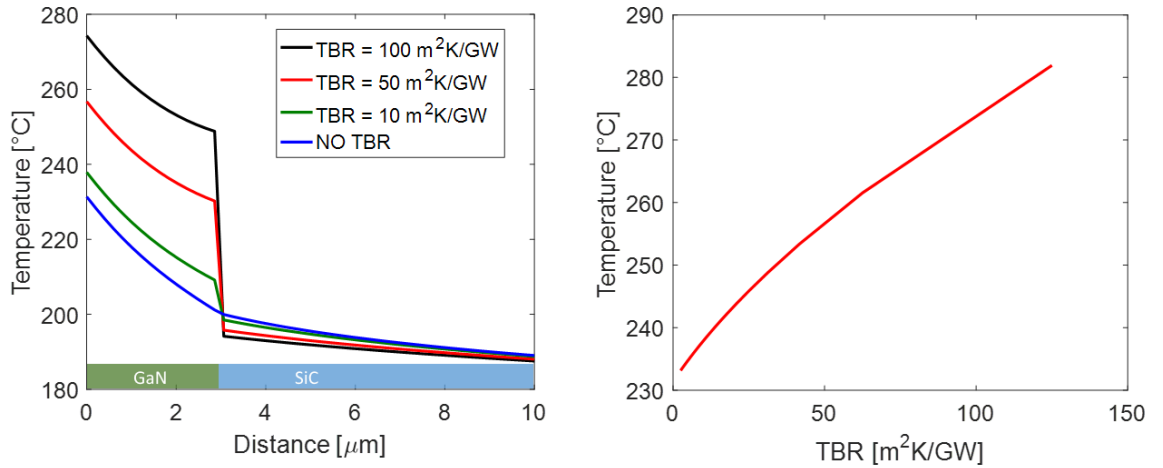


Figure 15. Maximum temperature of a GaN-on-SiC device as a function of TBR.

As has been demonstrated, reduction of the TBR is vital to improving device performance regardless of the substrate used. Chapter 2 will focus on basic understanding of phonons and some current methods used to estimate the TBR between two materials.

1.5 Research Objectives

Based on the information outlined above, significant effort is still required in order to properly understand the impact that interfacial layers have on the TBR in GaN based devices. This is especially important in GaN HEMTs where the extremely localized heat flux has been shown to cause significant device degradation. Unfortunately, bulk GaN substrates have not reached a level of maturity that allows for large area defect free wafers at a reasonable cost. For this reason, GaN HEMT devices are manufactured on non-native substrates that require additional interfacial layers in order to facilitate GaN growth that is sufficient for device implementation. The additional thermal impedance introduced through these layers can often be the limiting factor in the operational limits of the device. It is not enough to simply place a larger heat sink on the packaged device, as the thermal limitation due to TBR is present within a few microns of the device channel. This work will look specifically at the thermal and mechanical impact of interfacial layers for a series of GaN-on-Si material systems and devices. The primary research question addressed in this work is:

- **How does the inclusion of a superlattice (SL) structure impact interfacial heat transfer, performance, and reliability for a GaN-on-Si HEMT device?**

This question is addressed through the evaluation of residual stress in the GaN channel and buffer layer using photoluminescence (PL) and Raman spectroscopy. Followed by evaluation of the GaN thermal conductivity as a function of thickness and the effective GaN/Si TBR for a series of samples using TDTR. Finally, using Raman active nanoparticles the operating temperature of a series of devices is

measured and the through thickness temperature profile for SL and non-SL devices is demonstrated. An FEM model is developed to back up experimental observations.

This leads to the assumption that it may be possible to place a high thermal conductivity material such as diamond close to the heat source in the form of a heat spreader, or even incorporating the diamond as the device substrate. The effectiveness of CVD diamond device implementation is still under investigation and is a significant part of this work. This is accomplished by using experimental methods to measure the thermal properties of both bulk and thin film diamond materials that are grown on Si and GaN. A thorough analysis of the impact of dielectric layers on the TBR between GaN and diamond is presented to aid in the understanding of these interfacial layers. The use of high resolution imaging and elemental analysis are used to aid in the analysis. It is shown that simply measuring the TBR between materials is not sufficient to create a full understanding of thermal transport through the interface. Rather material characterization through high resolution imaging and elemental analysis are necessary to develop a more complete understanding of how interfacial layers impact heat flow through a material system such as GaN-on-diamond. Here, the primary research question that will be addressed is:

- **What is the role of small diamond grains and dielectric layers in limiting thermal transport in a GaN-on-diamond device and across the interface of a GaN/diamond material system?**

This question is addressed through the measurement of bulk and thin film diamond thermal conductivity using TDTR. This is carried on suspended membrane samples in order to isolate in-plane thermal transport. A careful study that looks at the non-homogeneous thermal conductivity due to grain boundaries in a bulk diamond

sample is presented by altering the spot size of the TDTR measurement. Additionally, thorough interface characterization of GaN-on-diamond samples with different dielectric layers is performed through a combination of TDTR, SEM/TEM imaging, and elemental analysis using EELs.

Finally, as mentioned bulk GaN substrates are still limited in their size and quality, leading to a costly implementation when using in transistor and diode devices. This technology, however, is extremely important to pursue in order to fulfill the full spectrum of electronic devices that are possible with GaN materials. Current limitations in creating vertical transistors based on bulk GaN were previously discussed, but there has been significant progress recently in the creation of vertical GaN-on-GaN diode structures. While still in their infancy, these GaN based diodes appear to offer significant advances in terms of size, efficiency, and power handing capabilities for power electronic devices. Here, we fabricate and evaluate vertical GaN-on-GaN diodes through a series of electrical and thermal testing. The thermal conductivity is shown to be impacted significantly by p-type doping that is required to create the PN junction in the diode. Additional transient thermal analysis demonstrates the importance of this non-homogeneous thermal conductivity in fully understanding the thermal operational limitations inherent in such a device. For this study, the primary research question is:

- **How does device passivation impact thermal/electrical performance for GaN-on-GaN PN diodes and how does the additional doping required impact the thermal performance of the device?**

This question is addressed by fabricating two sets of PN diodes that are identical except for an additional polyimide passivation layer on one of the dies. The two

sets are subject to a series of electrical testing to show difference in performance which is then followed by EL imaging that is used to explain differences in the performance curves. Thermal analysis is performed with TDTR in order to measure the thermal conductivity of the GaN as a function of thermal penetration depth. Finally, a transient thermal analysis is performed using a TTI approach that is used to evaluate the thermal impact of device operation. An FEM model is developed in order to back up experimental observations and provide additional insight into device limitations.

The above questions and issues will be addressed throughout this dissertation, with an overall outline of each chapter and its contribution to the overall understanding of the document outlined below in Section 1.6

1.6 Dissertation Outline

Chapter 2: introduces the reader to concepts and terminologies used throughout the dissertation. A portion provides an understanding of basic phonon transport as it is currently understood, with specific sections that focus on the approximations and models that are used to understand and estimate how heat/phonons transport across interfaces. This is discussed through the concept of phonon dispersions, density of states, and current analytical and numerical methods used to approach interfacial heat transfer.

Chapter 3: discusses the experimental methods used throughout the dissertation. Optical non-intrusive methods to measure both temperature and stress are presented by introducing the concept of Raman thermography and photoluminescence (PL). This is followed by a detailed description of time-domain thermoreflectance (TDTR). The theory

and instrumentation of the system is provided, followed by a basic mathematical derivation of the equations necessary to solve the heat equation and interpret the electronic signal. An understanding of TDTR sensitivity and uncertainty estimation is then presented.

Chapter 4: provides a complete study of a series of GaN-on-Si wafers and devices that is aimed at answering the previously mentioned research question. The experimental methods described in Chapter 3 are employed to provide experimental measurements of the residual stress in a GaN channel with and without a SL transition layer, this measurement is then used for an additional estimation of stress in the AlGaIn device layer. The thickness dependent thermal conductivity of GaN is measured from a series of samples with increasing GaN thickness and the TBR between GaN/Si is evaluated for GaN grown on an AlN only transition and GaN grown on a SL transition. Device temperature rise is measured using Raman thermography and it is demonstrated how the SL layer and GaN thickness impact the temperature profile in each device layer.

Chapter 5: provides insight into the thermal conductivity of bulk CVD diamond and thin diamond films using TDTR to measure bulk samples and thin films. Multiple bulk samples are measured and compared among different laboratories and methods. Measurements of the non-homogenous thermal conductivity due to diamond grains is carried out by adjusting the spot size of the TDTR measurement. Thin diamond membranes are measured in order to isolate the in-plane thermal conductivity. A complete study of the impact of dielectric layers on thermal transport in GaN-on-diamond devices is carried out using TDTR, high resolution imaging, and elemental analysis. Three separate samples are studied that consist of either no interlayer, or an AlN or SiN dielectric interlayer.

Chapter 6: looks at the impact of passivation layers on the electrical/thermal performance for a set of GaN-on-GaN vertical diodes. Two sets of identical diodes are fabricated and only one is subject to a polyimide passivation. Electrical measurements are used to show the diode performance, which are followed by EL imaging that provides additional insight into the differences seen in the electrical performance. TDTR is used to evaluate the impact of p-type doping on the thermal conductivity of the GaN in the drift region of the diode. Transient thermal imaging allows for a full field view of the temperature distribution of the measured diode as well as provide information about the transient thermal time constant in the device. An FEM model is used to provide further insight into thermal device limitations when operating under a pulsed condition.

Chapter 7: concludes the work and provides a summary and future recommendations.

CHAPTER 2. THEORY AND CONCEPTS OF INTERFACIAL HEAT TRANSPORT

2.1 Phonons

In a crystalline solid atoms are arranged in preferential structures. The arrangement of the atoms in a crystalline material is referred to as a crystal lattice. This lattice is a periodic structure that can be completely defined by a unit cell. A unit cell is a region of space that completely defines the crystal lattice such that when identical unit cells are placed next to each other in all directions it completely reconstructs the full structure. There also exists the primitive unit cell used to define the smallest possible region that completely defines the lattice. In order to better understand how thermal energy is transported through materials and interfaces it is often the case that atoms and their neighbors are considered spring mass systems. In this approximation the oscillation of atoms around the equilibrium positions has an important influence on energy transport and storage. The oscillations give rise to elastic waves that propagate energy through a material. These waves are referred to as phonons in the classical sense and exist as wavepackets that carry energy through the lattice.

Quantum mechanically the energy packets transmitted by the waves in the form of phonons are represented as quantized lattice vibrations and for a given frequency, ω , the smallest discrete value of the energy of a phonon is $\hbar \omega$, where \hbar is the reduced Planck's constant and ω is the phonon frequency. In this sense, phonons are considered discrete particles that carry energy and are also often referred to as quasi-particles or a quanta of lattice vibrations because they display both particle and wave behavior.

2.1.1 Phonon Dispersions

The relationship between the vibration frequency and the phonon wavevector is referred to as the phonon dispersion. This is realized by considering the mass of each atom and the interatomic force between them as simple springs. A common example of such a system is presented in Figure 16 for a diatomic chain of linear spring-mass arrays. For this example, it is assumed that the spring constant, K , is the same, however in most real solids this is not the case. The spring assumption is only a representation of the attractive and repulsive force between the atoms and is assumed to be linear when the displacement is sufficiently small. At high temperatures however, anharmonic oscillations may become significant, and the linear assumption is no longer valid. This model also assumes that the forces on atoms only come from their nearest neighbor.

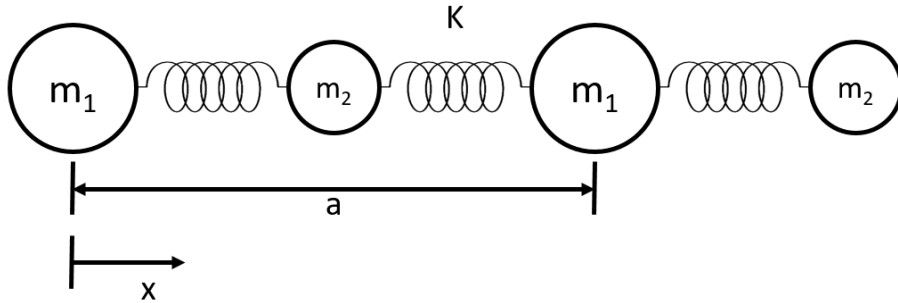


Figure 16. A 1D diatomic chain of atoms with different masses that are linked by springs with the same constant, K . This is the schematic used to formulate the equations of motion that will define the allowed vibrational frequencies in a crystal.

The solution to the system of equations that are derived from the spring-mass array presented in Figure 16 has been well documented in textbooks [55], and takes the form

$$\omega^2 = K \left(\frac{1}{m_1} + \frac{1}{m_2} \right) \pm K \left[\left(\frac{1}{m_1} + \frac{1}{m_2} \right)^2 - \frac{4 \sin^2 \left(\frac{ka}{2} \right)}{m_1 m_2} \right]^{\frac{1}{2}} \quad (1)$$

Equation 1 provides a relationship between the phonon frequency ω , and the wave vector k . Here $k = 2\pi/\lambda$, where λ is the phonon wavelength and is limited by the distance a , such that $2a \leq \lambda < \infty$. Because the solution is periodic in nature, the dispersion curve is plotted only within the first Brillouin zone. The Brillouin zone is defined based upon the primitive cell and a full discussion of the concept of reciprocal space and Brillouin zones is outside the scope of this thesis but has been exhaustively covered in textbooks and any solid-state physics course [89]. What is important here is that the resulting $\omega - k$ curves are the dispersion relations and when the unit cell consists of multiple atoms with different masses and different interatomic potentials two distinct branches are formed. Figure 17 shows a simple phonon dispersion for the system shown in Figure 16. The upper branch corresponds to the plus sign solution of Equation 1 and is referred to the optical branch because it is most important for infrared activities in ionic solids, while the branch that corresponds with the minus sign of the solution is referred to as the acoustic branch. In the acoustic branch the atoms move in phase with each other and are characteristic of traditional sound waves [55].

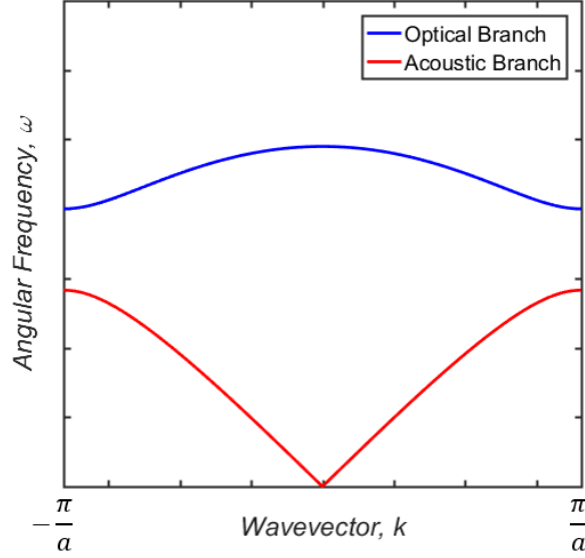


Figure 17. Phonon dispersion of a linear diatomic chain of atoms with the same spring constant K , as calculated by the nearest-neighbor model. Solution is constrained to the first Brillouin zone.

Calculation of phonon dispersions has been extended to a more realistic 3D system in which the lattice vibrations can now have both transverse and longitudinal modes. The different modes arise dependent upon how many atoms are in the primitive unit cell and are unique for all crystalline solids. In the specific case of GaN, the primitive wurtzite unit cell consists of two gallium atoms and two nitrogen atoms. This gives rise to a much more complex dispersion curve that must consider multiple directions and all modes of acoustic and optical phonons. A complete description of the phonon dispersion of GaN is beyond the scope of this thesis, however, as a comparison the phonon dispersion of wurtzite GaN is provided from literature in Figure 18 [90].

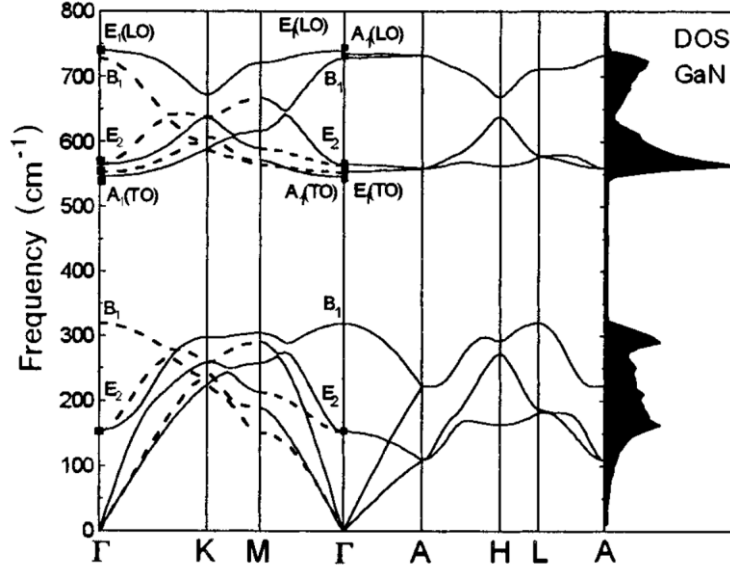


Figure 18. Full calculated phonon dispersion for bulk wurtzite-type GaN along with the associated density of states [90].

The slope of the dispersion curve gives the group velocity of each phonon mode as

$$v_g = \frac{\partial \omega}{\partial k} \quad (2)$$

where the group velocity is representative of the speed at which the phonon wavepackets propagate in the crystal. Phonons with a steep slope will transport energy faster than those with a shallower slope. Understanding of how much energy can be transferred in the crystal for phonon mode is inherent to the phonon density of states (DOS). It is defined as the number of modes per unit frequency per unit volume of real space, or the number of energy states that are available for occupation in a solid. Mathematically it is defined in 3D k -space as

$$D(\omega) = \frac{1}{(2\pi)^3} \frac{dk}{d\omega} \quad (3)$$

where $d\mathbf{k} = dk_x dk_y dk_z$, in order to consider all directions [55]. The DOS is a function of the inverse slope of the phonon branches as can be seen in Figure 18. These calculations can quickly become very complex and often require numerical methods in lieu of a closed form solution [91]. Section 2.2 will discuss interfacial thermal transport and expand upon the Debye approximation that is often implemented when calculating phonon contributions to heat capacity, thermal conductivity, and interfacial phonon transport.

2.2 Interfacial Thermal Transport

As the miniaturization of electronics continues to be at the forefront of the semiconductor industry, understanding of thermal transport across interfaces of dissimilar materials that are in atomically intimate contact has become an ever-pressing issue. With increased heat dissipation per unit volume and epitaxial growth of thin films, devices are now seeing operational limitations due to their inability to effectively remove the heat from the source generation in the material. Increased thermal resistances in devices have been shown to come from a reduction in a materials size dependent thermal conductivity [92] as well as a significant contribution attributed to the TBR at the interface between two material systems. This section will further explore current analytical and computational methods that are being used in order to predict the TBR between two materials based on their phonon dispersions.

2.2.1 The Debye Approximation

A common simplification of the phonon dispersion is the Debye approximation. This approximation implies that the medium is isotropic and in all directions the phonon branches have the same speed. It is also assumed that there is a linear relation between the

frequency and wavevector. In this case the group velocity of phonons as described in equation 2 simply becomes:

$$v_D = \frac{\omega}{k} \quad (4)$$

this assumption dramatically simplifies the phonon DOS as described by equation 3 and allows for a simple parabolic solution in the form of:

$$D(\omega) = \frac{3\omega^2}{2\pi^2 v_D^3} \quad (5)$$

these assumptions have been shown to be valid in situations where the heat transport is dominated by low frequency phonons. Figure 19 shows the Debye dispersion for a simple 1D atomic chain as compared to the dispersion calculated from solving the equations of motion mentioned in Section 2.1.1 and the phonon DOS using the Debye approximation for aluminum as compared to values measured in literature [93].

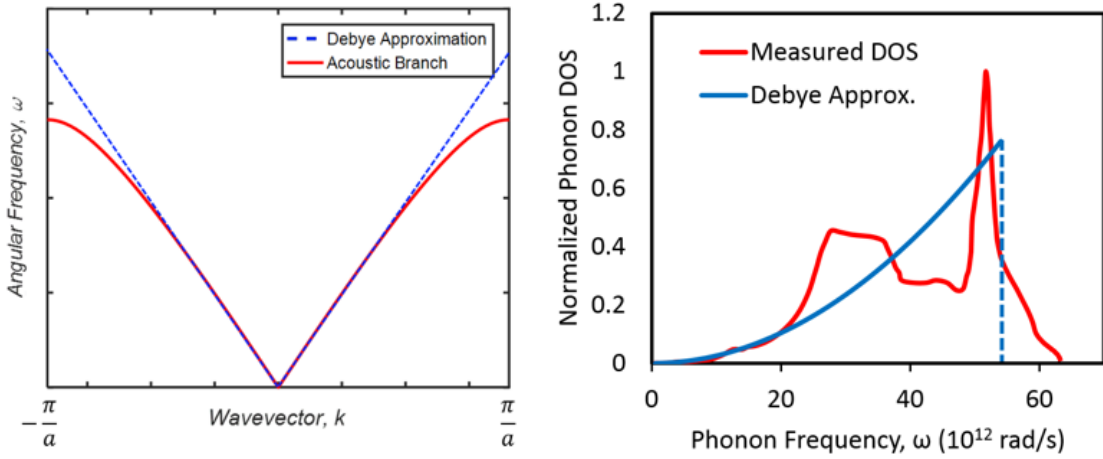


Figure 19. (Left) Comparison of a simple phonon dispersion for a 1D atomic chain to that of the Debye approximation. (Right) An actual phonon DOS for aluminum as measured in literature [93] compared to a phonon DOS using the Debye approximation.

The Debye approximation does not accurately represent real phonon dispersions at the zone edge where the wavevector flattens out. It is also not suitable to represent contributions of optical phonon modes. In order to correctly implement the Debye approximation a cutoff wavevector must be defined such that at the boundary of the Brillouin zone $k_D = \pi/a_D$, where k_D is the Debye cutoff wave vector and a_D is the lattice constant. These approximations are important when computing a materials specific heat, thermal conductivity, and in the interface thermal transport models that will be described in Sections 2.2.2 and 2.2.3.

2.2.2 Diffuse Mismatch Model

Under the assumption of atomically intimate contact between two materials a model to estimate the TBR due only to phonon transmission at the interface was originally developed by Swartz and Pohl [94] and is known as the diffuse mismatch model (DMM). This model assumes that phonons will scatter at an interface according to a probability that

is determined by the phonon dispersions of the two materials. However, in this model the scattering is assumed to be diffuse and elastic. In other words, the phonons from one material that imping at the interface of the two materials will scatter and lose all memory of their origin while maintaining their frequency. At the interface the phonons will either transmit or reflect, with the probability for transmission being only a function of the materials phonon DOS. In this model, a phonon moving away from the interface does not ‘know’ whether it as a transmitted or reflected phonon. It is only required that the total number of reflected and transmitted probabilities from a material add up to unity (i.e. $T_{12} + R_{12} = 1$). Mathematically the TBC across an interface can be given by

$$h_K = \sum_j \int_0^{\omega_{max,j}} \frac{\partial q_{1,j}(\omega)}{\partial T} \Gamma_{1 \rightarrow 2}(\omega) d\omega \quad (6)$$

where ω is the phonon angular frequency, $\Gamma_{1 \rightarrow 2}$ is the phonon transmission coefficient, $q_{1,j}$ is the phonon heat flux from side 1 with polarization j . $\omega_{max,j}$ is the maximum phonon angular frequency in branch j , and T is the temperature at the interface. Here the heat flux due to each phonon branch, j , is summed together to provide the total TBC across the interface. The phonon heat flux derivative is defined as:

$$\frac{\partial q_{1,j}(\omega)}{\partial T} = \frac{1}{4} \hbar \omega D_{1,j}(\omega) v_{1,j}(\omega) \frac{\partial f(\omega)}{\partial T} \quad (7)$$

where \hbar is the modified Plank constant, $f(\omega)$ is the Bose-Einstein distribution at equilibrium, $D_{1,j}(\omega)$ is the phonon DOS in side 1 for the phonon branch, j , and $v_{1,j}(\omega)$ is the group velocity of phonons in side 1 from branch j . As is evident from equation 6 and equation 7 knowledge of the DOS and phonon dispersions are necessary in order to

calculate the TBC across the interface. Due to the complexity of these dispersions the previous discussed Debye approximation is often used to define the maximum phonon angular frequency and allow for a linear relationship between the group velocity and the wavevector. This assumption also negates any contributions due to optical phonon branches. The significant factor in equation 6 is indeed the transmission coefficient $\Gamma_{1 \rightarrow 2}$, and it is defined as:

$$\Gamma_{1 \rightarrow 2}(\omega) = \frac{\sum_j [k_{j,2}(\omega)]^2}{\sum_j [k_{j,2}(\omega)]^2 + \sum_j [k_{j,1}(\omega)]^2} \quad (8)$$

Equation 8 effectively defines the ratio of energy that is capable of travelling from interface 1 to 2 by considering the fully elastic limit where a phonon can only transmit to material 1 to 2 if there exists a phonon mode of equivalent energy in material 2 regardless of polarization. The phonon transmission probability is therefore only a function of the dispersion relation. When the Debye approximation is applied these equations are readily solved. Under these assumptions, the DMM has often been shown to under predict the TBC for many material systems [95, 96]. However, there have been many modifications to the DMM that account for full phonon dispersions [97], inelastic scattering [98], optical phonon modes [95], disordered interfaces [99], and surface roughness [100]. Appropriate modifications have shown significantly better agreement to measured values, but these are often for very specific material systems and do not provide a means to fully account for phonon interactions at an interface. More rigorous computational methods such as molecular dynamics (MD), lattice dynamics, and first principle simulations have been used

extensively, however, for many materials accurate knowledge of interatomic potentials creates significant limitations in the accuracy of the computation [101-104].

2.2.3 *Acoustic Mismatch Model*

Analogous to the DMM there exists a model that considers the idea that at an interface between two dissimilar materials the differing densities and sound speeds give rise to a mismatch in acoustic impedances. Appropriately named the acoustic mismatch model (AMM), it also generally follows the Debye assumptions that the velocities for all polarizations are the same, and a linear phonon dispersion is considered [105]. The methodology is similar to that of the DMM with the significant difference coming from the definition of the transmission coefficient. Here the transmission only considered longitudinal phonons and relies on Snell's law [106] to incorporate the incident angle of the phonon propagation direction. It is typically defined as:

$$\tau = \frac{4z_{A1}z_{A2}\cos\theta_1\cos\theta_2}{(z_{A1}\cos\theta_1 + z_{A2}\cos\theta_2)^2} \quad (9)$$

Where $z_{A1} = \rho_1 v_1$ and $z_{A2} = \rho_2 v_2$ with ρ as the density, v as the velocity, and θ is the angle between the normal direction and the incident phonon propagation. It should be noted that the transmission does not rely on particular phonon frequencies but considers a single Debye velocity for each material is related only to the longitudinal acoustic phonon mode. This model has been shown to be valid at low temperatures when long wavelength phonons are dominant but generally falls short at temperatures greater than 30K [94].

2.2.4 Interface Conductance Modal Analysis

Recent work from Gordiz *et al.* has introduced a new formalism for understanding interfacial thermal transport. The interface conductance model analysis (ICMA) is an MD approach that distinguishes itself from other methods by allowing for calculation of the modal contributions to the thermal interface conductance. This method provides a more complete understanding of modal contributions at the interface by including full anharmonicity. Using an Si-Ge interface they have been able to show excellent agreement with experimental observations in literature using the ICMA method [107].

CHAPTER 3. CHARACTERIZATION METHODS

3.1 Raman Spectroscopy

3.1.1 Introduction

Raman spectroscopy is a well understood technique that is capable of observing optical phonon vibrational modes through inelastic scattering of a monochromatic light source upon interaction with phonons in a crystal lattice. This method has been discussed in great detail elsewhere [108], and will only briefly be described here. As photon energy is absorbed, atoms in the crystal lattice experience changes in the vibrational energy of their phonon modes. While most atoms scatter at the same energy as the original excitation (Rayleigh scattering) a select few (~ 1 out of 1×10^8) do not return to their original state and emit a photon at a wavelength proportional to the difference between their virtual energy state and the original energy state. This is referred to as Stokes scattering [109]. This phenomenon is detected using a spectrometer and active Raman modes are identified by their peak position. Because the location of the peak position is related to the interatomic potential between atoms, a shift in a given Raman mode can be influenced by changes in strain and temperature [110]. Measurements of both temperature and stress in GaN HEMTs using Raman methods have been investigated extensively [111-113].

3.1.2 Thermal Metrology

Using Raman peak shifts, approximate temperature changes can be deduced with a spatial resolution of $\sim 1 \mu\text{m}$ and a temporal resolution of $\sim 3^\circ\text{C}$ [114]. Raman has been used to estimate the TBR in GaN HEMT structures by mapping a Raman temperature profile

leading out of a device channel or a TLM structure [87]. By doing this, it is possible to see how the temperature decays as the probe is moved away from the active channel. This temperature map is then combined with an model using a finite element method (FEM) in which thermal properties are varied in order to provide the best fit to the experimental data. A distinct advantage of using a steady state method such as this stems from the fact that knowledge of the density and heat capacity of the layers of interest does not need to be known, as these parameters can cause large uncertainty in transient measurements.

Because GaN is transparent to a typically used 532 or 488 nm wavelength laser it is often possible to observe Raman modes of multiple materials in a GaN HEMT system [87]. By knowing the experimental temperature gradient, it is possible to use both analytical [86] and numerical solutions [87], that are appropriate to the device geometry, to fit for parameters such as TBR or thermal conductivity. Using a numerical approach with Raman measurements Saura *et al.* found the TBR for both a GaN/SiC and GaN/Si interface to be 33 m²K/GW [87]. Manoi *et al.* has measured values ranging between 15 to 50 m²K/GW using this approach for GaN/SiC interfaces [84]. A transient approach using Raman thermometry from Kuzmik *et al.* Estimated a TBR of 70 m²K/GW for GaN/Si and 120 m²K/GW for GaN/SiC [115]. Pomeroy *et al.* used a Raman mapping technique similar to Saura *et al.* in order to obtain the TBR between GaN and diamond. They find a TBR of 27 m²K/GW for GaN/diamond interface with a 25 nm dielectric interlayer [116]. While Raman has been shown to provide fairly accurate temperature estimates, it is difficult to use as a tool to extract thermal properties due to its sampling size, stress influences, and the need for an accurate system model. Often, devices have different types of interlayers

depending on the manufacturer, and thermal property assumptions in the model can lead to large errors [117].

3.2 Photoluminescence Spectroscopy

3.2.1 Introduction

Similar to Raman spectroscopy, Photoluminescence (PL) spectroscopy uses a monochromatic light source (typically a laser) as a contactless, non-destructive method to probe the electronic structure of a material. Where-as in the case of Raman, it is the vibrational phonon properties that are being probed. In a typical use of PL, a monochromatic laser line is directed onto a sample. The light energy is then absorbed into the material where it elevates carriers in the valence band to the conduction band by promoting electrons to permissible excited states. Once promoted, the electrons seek to return to their ground state by dissipating the excess energy. One way this energy is removed from the material is through the emission of light, this is considered a radiative process typically referred to as luminescence or fluorescence. When photons are used to create this excitation and subsequent emission, the process is referred to as PL. There also exists non-radiative processes that are the result of energy exchange within the conduction band and do not result in light emission. Figure 20 provides an illustrative example of the PL process. The energy of the emitted light due to the fluorescence is directly related to the electronic bandgap of the material.

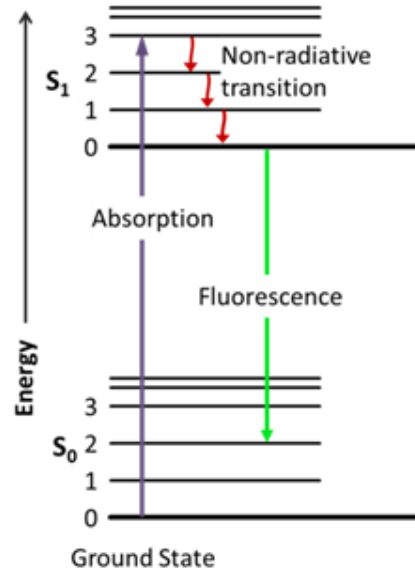


Figure 20. PL process demonstrating the promotion of electrons through an absorption process that is due to photo excitation and the subsequent non-radiative transitions and fluorescence emission [118].

3.2.2 Stress Metrology

A materials bandgap is a result of the interatomic distance between atoms in the crystal lattice as well as the potential energy that binds those atoms. Because of this, changes in a materials bandgap can be directly related to changes in the stress state of that material. Specifically, for GaN, an increase in tensile stress will result in a reduction of the materials bandgap energy (often referred to as a red shift), while an increase in compressive stress will cause an increase in the bandgap energy (or a blue shift). In order to probe GaN with PL an excitation source that has an energy larger than the bandgap is required to induce the electron excitation from the valence to the conduction band. Because of this evaluation of the stress by PL is constrained to the small absorption depth of the laser at the excitation wavelength. In our case a 325 nm laser line is used which results in an

absorption depth of approximately 80-90 nm [119]. This means that when using a 325 nm laser to probe the stress state of GaN, we are only obtaining the stress near the surface of the material. Other methods using Raman spectroscopy are able to obtain a through thickness average of stress [113]. However, when considering an AlGaN/GaN HEMT, we are often more concerned with the stress present in the AlGaN and therefore a near surface GaN measurement allows us to more accurately estimate the stress in the AlGaN as will be discussed further in Section 4.2.1. In order to accurately determine the state of stress using PL a proper correlation between the bandgap energy and the change in stress must be determined. Often a “stress-free” reference of bulk material is used to determine the “stress free” bandgap energy and then applied to a linear assumption that the change in energy from the “stress-free” reference is correlated to the stress through a biaxial stress conversion coefficient [113]. However, bulk GaN can be grown using several different methods as previously discussed, each of which results in their own unique set of defects in the material and as a consequence differing states of stress and bandgap energy. For this reason, it may not be practical to assume a sample of bulk GaN grown by different means than that of an epitaxial layer can be directly related in terms of a “stress-free” reference. A detailed study by Choi *et al.* combined x-ray diffraction (XRD) to determine the lattice spacing and PL measurements to determine the bandgap energy over multiple samples that spanned from a compressive to tensile stress state [113]. Through comparison of lattice constants and bandgap energy they were able to determine where the strain-free lattice constant existed and through conversion of strain to stress using an elastic modulus [120], able to develop a proper coefficient relating the change in bandgap energy to stress. While this seems to be an effective approach, there is still much discrepancy in the literature

regarding “stress-free” reference values and proper coefficients relating PL measurements to stress [121]. However, for the purposes of this thesis, we will follow the approach used by Choi *et al.* [113]

3.3 Time-domain Thermoreflectance (TDTR)

3.3.1 Introduction and Theory

Measurement of thermal properties using an optical pump-probe technique is based on the simple idea that changes in a materials temperature are directly related to changes in a materials reflectance. For small temperature excursions the change in reflectance can be assumed to be linearly proportional to the surface temperature of the material. This is often expressed as:

$$\frac{\Delta R}{R} = \left(\frac{1}{R} \frac{\partial R}{\partial T} \right) \Delta T = C_{th} \Delta T \quad (10)$$

where, C_{th} is the thermoreflectance coefficient with units of $^{\circ}\text{C}^{-1}$ and represents the change in reflectance as related to temperature. In a pump-probe configuration, the pump beam acts as the heater with the probe beam acting as a thermometer by relaying information about the reflectance change of the material.

TDTR is an optical technique that splits a pulse from a femtosecond laser onto a pump and probe path. The pulse directed down the pump path is used to periodically heat the sample, while the pulse of the probe path is delayed by a mechanical stage and used to measure the transient temperature decay of the sample surface via a change in reflectivity. A thin aluminum transducer (~ 90 nm) is deposited onto the surface to absorb the laser

energy and provide the thermorefectance signal via a photodiode connected to a lock-in amplifier. A radially symmetric model of heat diffusion through multiple layers is then used to fit thermal parameters to the experimental data [122]. Several key advantages of TDTR include its use of a femtosecond laser, this allows for time delays less than 1 picosecond. The ultra-high temporal resolution of TDTR has allowed for the study of non-equilibrium dynamics involving energy carriers and coherent phonons [123]. In addition, the spatial domain through which the sample is probed can be adjusted based on the modulation frequency of the pump beam. By changing the frequency, the thermal penetration depth that is sampled in the material can be altered, which allows for the user to adjust frequencies in order to increase the sensitivity of desired thermal parameters such as the TBR between thin films. A significant draw back to the TDTR method lies in the costly and complex setup.

3.3.2 *Instrumentation and Optics*

While the idea of pump-probe thermorefectance has been used since the mid 1980's [124], there have been many significant advancements in instrumentation and system configurations since that time [122, 125-128]. Currently, there are two popular variations of the TDTR implementation, the double color [129] (as used in this work) and the two-tint arrangement [128]. The two-tint arrangement uses sharp edge filters in order to separate the pump and probe beams, while the double color arrangement uses a bismuth borate (BiBO) crystal to convert the initial laser wavelength of 800 nm red light to 400 nm blue light in order to allow for proper filtering and isolation of the pump and probe beams along the detection path of the system. Both variations utilize the same electronic detection methods and the same thermal model in the post processing.

Our implementation of TDTR consists of a Ti:Sapphire laser (Spectra Physics Mai-Tai HP) that oscillates at 80.7 MHz with an energy of ~ 40 nJ/pulse and a pulse width of ~ 150 fs, resulting in an average power of ~ 3 W at a wavelength of 800 nm. The source beam from the laser is passed through an optical isolator (ConOptics Model 714) that ensures back reflections do not enter the laser cavity. Then polarizing optics are used to split a portion of the laser power down a pump and probe path. The pump path uses an electro-optic modulator (ConOptics Model 160) that is controlled by a function generator (Stanford Research Systems SSR850) to chop the pulse train at a specific frequency (between 1.2-11.6 MHz for our implementation). Frequency doubling is then achieved using a BiBO crystal resulting in a wavelength of 400 nm. Additional collimating optics are then used to control the size of the pump beam as it is directed onto the sample. The probe beam remains as 800 nm light and is first expanded before being directed onto a motorized delay stage. We use a double pass delay stage which allows for probe delay times relative to the pump of up to 7 ns. By expanding the probe beam as it passes through the delay stage and then compressing the beam after the stage, we are able to reduce any divergence of the probe at long delay times. Both the pump and probe beam are then directed onto a collinear path where they impinge on the sample. Because we are only interested in the signal measured by the probe beam, the reflected beam is directed normal to the incident impingement and is filtered out from the pump beam through the use of dichroic mirrors and bandpass filters. This ensures that only the 800 nm probe light is measured by the photodetector. A detailed schematic of the TDTR system used in this work is shown in Figure 21.

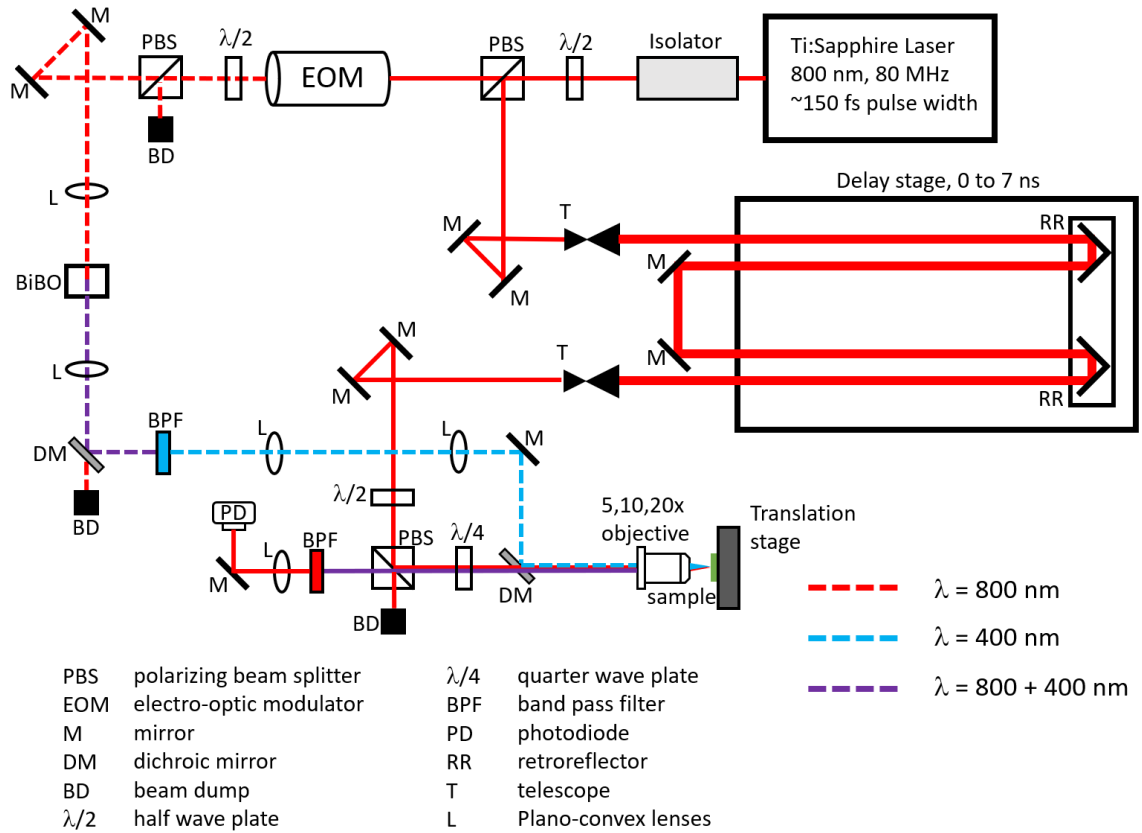


Figure 21. Detailed schematic of TDTR system.

A high-speed PIN diode (Thorlabs DET10A) is used to convert the photons into an electrical signal. This detector is coupled to an inductor, creating an RLC circuit. The inductor chosen in conjunction with the frequency that is prescribed to the EOM by the function generator. This amplifies the signal at the specific frequency and acts as an electronic bandpass filter that minimizes higher harmonics [130]. The signal from the detector is further amplified using a high-speed low-noise electronic amplifier (Stanford Research Systems SR445a), which can increase the gain up either 5x or 25x by using multiple stages, however, this comes at a cost of increased electronic noise. The electronic signal is then routed to a lock-in amplifier (Stanford Research Systems SR844) which detects the phase and amplitude of the measured signal as compared to the reference signal prescribed by the

function generator. The lock-in amplifier is connected to a data acquisition system and the in-phase and out-of-phase components of the signal are acquired in reference to the delay time of the probe beam. The phase shift due to the measurement system is accounted for by adjusting the phase of the lock-in amplifier such that the out-of-phase signal remains constant through a zero delay time [122]. An illustrative example of a traditional sample with the substrate, thin film, and transducer along with the heating from the pump beam is shown in Figure 22 alongside the thermal response due to the pump excitation and the subsequent delay of the probe.

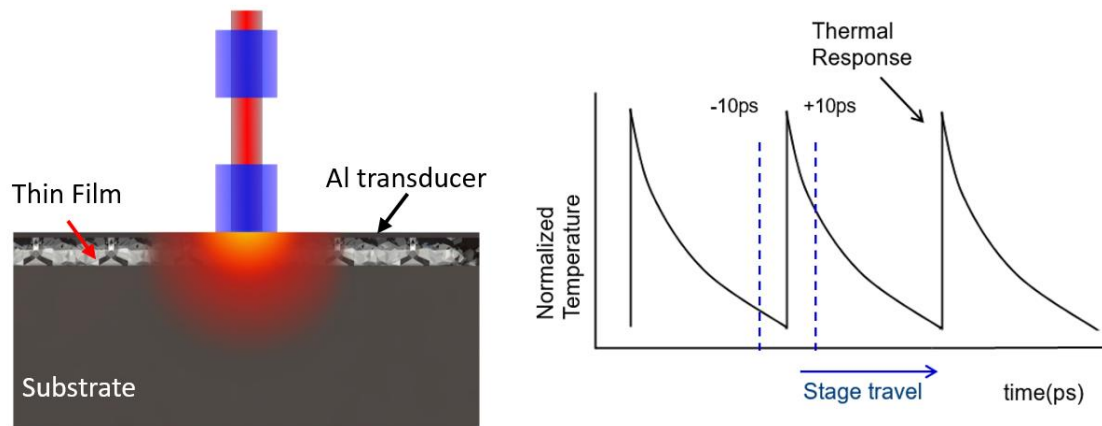


Figure 22. (Left) A typical sample configuration measured with TDTR. In this case a thin diamond film is represented, however this film can consist of a broad range of materials. The period pump heating creates a thermal wave in the material after being absorbed by the transducer. (Right) Representation of the thermal response of the material and the probe delay relative to the stage travel.

Appropriate samples for TDTR normally consist of bilayer or trilayer systems, with the thin films in a trilayer system on the order of 100's of nm to a few microns. The exact ability to measure thin films relies heavily on the thermal properties of the film itself. Because TDTR is a transient method, accurate knowledge of the volumetric heat capacity for the materials is often required, and TBC between each interface in the system must be

considered as well. As mentioned, the depth dependence of the measurement is typically limited by the thermal penetration depth, given by [122]:

$$\alpha = \sqrt{\frac{\kappa}{C_v \pi f}} \quad (11)$$

where α is the thermal penetration depth (m), κ is the thermal conductivity (W/m-K), C_v is the volumetric heat capacity (J/m³K), and f is the frequency (Hz). This estimates the depth of the thermal wave and is indicative of how much of the material is sampled using a specific frequency with TDTR. Although recent work by Braun *et al.* has shown that this relationship may not always be fully indicative of the sampling depth and in some cases a more rigorous approach such as numerical modeling is needed [131].

3.3.3 Heat Transfer Analysis and Electrical Response

A general multilayer model to describe the frequency domain response to a pulsed Gaussian heat flux on the surface of a material system specifically for TDTR was first published in detail by Cahill *et al.* [122] and has since seen a number of adaptations to account for anisotropic conduction [129], bi-directional conduction [132], offset laser spots [133], and optical absorption [134] have been implemented. Additionally an explicit solution for a three layer system has been provided by Lui *et al.* [135]. Rather than rehash all of the aforementioned solutions, this section will focus on providing the basic insight and significant equations and transforms needed to solve relate the variation in sample surface temperature to the material properties by solving the heat diffusion equation in a

multilayer structure. We will then derive the lock-in amplifier response as related to the thermal response through a transfer function.

The use of a transfer function is common in many types of controls and signal processing applications where it is necessary to relate electronic signals as an output to specific systems inputs [136]. Specifically, linear time invariant (LTI) systems are common in that for these systems, the input and output scale proportionally and they possess the property of superposition, where the system response to multiple inputs is simply the sum of all the individual inputs. When considering conduction heat transfer, this assumption is valid only if the temperature changes of the system are small enough such that the thermal properties of the system are considered to be constant [137]. The thermal response due to the laser heating in a TDTR system is such that thermal accumulation effects will quickly raise the material to a steady state temperature that is typically only a few °C and the thermal wave will then oscillate at a certain phase and amplitude around that temperature. The goal of the heat transfer analysis and the electrical response is to develop a transfer function that will relate the amplitude and phase of the oscillating wave to the electrical output of the lock-in amplifier. This is first achieved by solving the heat equation for a multilayer radial conduction system in the frequency domain and implementing the frequency response of the sample surface temperature to a transfer function that is weighted by the intensity distribution of the probe beam.

To do this we start with the simple relationship:

$$A(\omega_0)e^{i(\omega_0 t + \varphi)} = Z(\omega_0)e^{i\omega_0 t} \quad (12)$$

where, A is the amplitude and φ is the phase of the signal measured by the lock-in. These values will depend on the physical properties of the material system, the modulation frequency, and the time delay between the pump and probe pulses. The transfer function Z is a complex number that contains information about the thermal properties of the system and is related to the output for a reference wave at a given frequency by $e^{i\omega_0 t}$. Here, i is the imaginary number, ω_0 is the frequency of the reference wave, and t is the time. In the TDTR analysis this transfer function is given by the following [138]:

$$Z(\omega) = \beta \sum_{k=-\infty}^{\infty} H(\omega + k\omega_s) \exp(ik\omega_s \tau) \quad (13)$$

where $H(\omega + k\omega_s)$ is the frequency domain solution for the surface temperature, ω is the reference frequency of the EOM, ω_s is the frequency of the laser pulses (~ 80 MHz in this case), k is the summation variable, τ is the time delay between the pump and probe, and β is a constant give as:

$$\beta = \frac{1}{2} Q_{pump} Q_{probe} (1 - R_{\lambda pump}) \left(\frac{dR}{dT}_{\lambda probe} \right) G_{det} \quad (14)$$

here, Q_{pump} and Q_{probe} are the energy per pulse of the pump and probe respectively, $R_{\lambda pump}$ is the surface reflectivity of the at the pump wavelength, $\frac{dR}{dT}_{\lambda probe}$ is the thermorefectance coefficient at the probe wavelength, and G_{det} is the product of the photodetector gain and photodiode responsivity at the probe wavelength. Equation 14 contains the relationship of the thermorefectance coefficient and the input powers, however as we will find for most TDTR analysis these values do not impact the solution

due to taking signal ratios that allow them to cancel each other out. The main goal of our analysis is to find the surface temperature $H(\omega + k\omega_s)$ solution in the frequency domain.

Knowing the form of the equation, we can begin the heat transfer analysis from the basic governing heat equation in cylindrical coordinates:

$$\frac{\kappa_r}{r} \frac{\partial}{\partial r} \left[r \frac{\partial T(r, z)}{\partial r} \right] + \kappa_z \frac{\partial^2 T(r, z)}{\partial z^2} = C_v \frac{\partial T(r, z)}{\partial t} \quad (15)$$

Where r and z are the radial and cross-plane coordinate, respectively, t is the time, T is the temperature as a function of r and z , C_v is the volumetric heat capacity, and κ_r and κ_z are the respective in-plane and cross plane thermal conductivities. In order to solve equation 15 boundary conditions are applied that contain continuity of the layers and the heat source as a heat flux. They take the form:

$$T(0, r, t) = T_{top}; \quad \left. \frac{\partial T(z, r, t)}{\partial z} \right|_{z=0} = -\frac{1}{\kappa_z} q_{top} \quad (16)$$

$$T(L, r, t) = T_{bot}; \quad \left. \frac{\partial T(z, r, t)}{\partial z} \right|_{z=L} = -\frac{1}{\kappa_z} q_{bot} \quad (17)$$

$$T(z, r, 0) = 0 \quad (18)$$

where T_{top} and T_{bot} are the top and bottom surface temperatures and q_{top} and q_{bot} are the top and bottom heat fluxes, with the initial temperature set to zero since we are interested only the change of the surface temperature rather than the absolute temperature.

Hankel transforms are often used to simplify solutions with cylindrical symmetry. Here we will apply a zeroth order Hankel transform followed by a Fourier transform. This

will simplify the solution and transfer it from the time to the frequency domain. Details of the Hankel and Fourier transforms can be found in any graduate level textbook [139]. For brevity, the details of the transformations will not be expounded upon here, but others have gone through the solution in more detail [140]. Applying the transforms we can now rewrite the governing equation as:

$$-\kappa_r \chi^2 \Theta(z, \chi, \omega) + \kappa_z \frac{\partial^2 \Theta(z, \chi, \omega)}{\partial z^2} = C i \omega \Theta(z, \chi, \omega) \quad (19)$$

where χ is the Hankel transform domain variable, ω is the angular frequency, and Θ represents the temperature in Hankel space. In order to simplify the equation 19 further and apply the boundary conditions for a solution we define a new variable:

$$\mu = \frac{\kappa_r \chi^2 + i C \omega}{\kappa_z} \quad (20)$$

We can now rewrite equation 20 as:

$$\frac{\partial^2 \Theta(z, \chi, \omega)}{\partial z^2} - \mu^2 \Theta(z, \chi, \omega) = 0 \quad (21)$$

The form of the solution for equation 21 can take either exponentials or hyperbolic trig functions. We will use the hyperbolic functions here, which lead to a solution of the form:

$$\Theta(z, \chi, \omega) = A \cosh(\mu z) + B \sinh(\mu z) \quad (22)$$

with the constants A and B found by applying the boundary conditions. The new boundary conditions in considering the Hankel and Fourier transforms are identical to those in

equations 16, 17, and 18, with them as a function of χ and ω rather than r and t . Applying the boundary conditions the temperature and heat flux solution in Hankel space takes the form of:

$$\Theta(z, \chi, \omega) = \cosh(\mu z) \Theta_{\text{top}} - \frac{1}{\kappa_z \mu} \sinh(\mu z) \widetilde{q}_{\text{top}} \quad (23)$$

$$\widetilde{q}(z, \chi, \omega) = -\kappa_z \mu \sinh(\mu z) \Theta_{\text{top}} + \cosh(\mu z) \widetilde{q}_{\text{top}} \quad (24)$$

The two equations above give rise to a relationship between the temperature and heat flux at any point where $z < L$ in real space. When $z = L$ we have the condition where $\Theta(L, \chi, \omega) = \Theta_{\text{bot}}$ and $\widetilde{q}(L, \chi, \omega) = \widetilde{q}_{\text{bot}}$. We are then able to construct a transfer matrix that will relate the two quantities [137]:

$$\begin{bmatrix} \Theta_{\text{bot}} \\ \widetilde{q}_{\text{bot}} \end{bmatrix} = \begin{bmatrix} \cosh(\mu L) & -\frac{1}{\kappa_z \mu} \sinh(\mu L) \\ -\kappa_z \mu \sinh(\mu L) & \cosh(\mu L) \end{bmatrix} \begin{bmatrix} \Theta_{\text{top}} \\ \widetilde{q}_{\text{top}} \end{bmatrix} \quad (25)$$

The above result can then be generalized for multiple layers by multiplying matrices of each individual layer. In this case, L would now be equal to the thickness of the layer and is shown as:

$$\begin{bmatrix} \Theta_{\text{bot},n} \\ \widetilde{q}_{\text{bot},n} \end{bmatrix} = M_n M_{n-1} \dots M_{i+1} M_i \dots M_1 \begin{bmatrix} \Theta_{\text{top}} \\ \widetilde{q}_{\text{top}} \end{bmatrix} = \prod_{i=n}^{i=1} M_i \begin{bmatrix} \Theta_{\text{top}} \\ \widetilde{q}_{\text{top}} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} \Theta_{\text{top}} \\ \widetilde{q}_{\text{top}} \end{bmatrix} \quad (26)$$

Modeling of the thermal conductance between layers is achieved by setting the thickness of a fictitious layer to 0 and using the relation, $\widetilde{q}_a = h_{a,b}(\Theta_a - \Theta_b)$. Each matrix element in equation 26 contains the layer thickness, volumetric heat capacity and thermal

conductivities of the layer. Further simplification comes from the fact that most TDTR measurements will take place on a substrate that is thermally thick, therefore considered to be semi-infinite. In this case the heat flux at the bottom of the semi-infinite substrate is zero. If we apply this assumption, we can rewrite the matrix from equation 26 as:

$$\Theta_{top} = -\frac{D}{C} \widetilde{q_{top}} \quad (27)$$

The top surface boundary condition of $\widetilde{q_{top}}$ is dependent on the heating from the pump beam. The pump beam is assumed to have a Gaussian form dependent on the $1/e^2$ spot radius. A Gaussian intensity profile with unit power takes the form:

$$q_{top} = \frac{2}{\pi r_0} \exp\left(\frac{-2r^2}{r_0^2}\right) \quad (28)$$

where r_0 is the $1/e^2$ radius of the pump and r describes the radial dependence. If we take the Hankel transform of equation 28 we get:

$$\widetilde{q_{top}} = \frac{1}{2\pi} \exp\left(\frac{-\chi^2 r_0^2}{8}\right) \quad (29)$$

where we have now taken on the Hankel transform variable, χ in place of the radial dependence. In order to get the temperature in Hankel space we simply combine equations 27 and 29, which leads to:

$$\Theta_{top} = -\frac{D}{C} \frac{1}{2\pi} \exp\left(\frac{-\chi^2 r_0^2}{8}\right) \quad (30)$$

From here, the application of an inverse Hankel transform will bring the temperature solution back to real space:

$$T_{top} = \int_0^\infty k J_0(kr) \left(-\frac{D}{C}\right) \frac{1}{2\pi} \exp\left(\frac{-k^2 r_0^2}{8}\right) dk \quad (31)$$

where J_0 is a zero-order Bessel function of the first kind and k is the integration variable. To obtain our final solution we must consider that the measured surface temperature is weighted by the intensity distribution of the probe beam. In the case of coaxial beams, we can write an equation similar to equation 28 for the probe beam and include this weight in the measured temperature as:

$$H(\omega) = \int_0^\infty \left(\frac{2}{\pi r_1}\right) \exp\left(-\frac{2r^2}{r_1^2}\right) 2\pi r dr \int_0^\infty k J_0(kr) \left(-\frac{D}{C}\right) \frac{1}{2\pi} \exp\left(\frac{-k^2 r_0^2}{8}\right) dk \quad (32)$$

which can be simplified as a single integral over k .

$$H(\omega) = \frac{1}{2\pi} \int_0^\infty k \left(-\frac{D}{C}\right) \frac{1}{2\pi} \exp\left(\frac{-k^2 (r_0^2 + r_1^2)}{8}\right) dk \quad (33)$$

Finally, this equation is solved numerically using software such as MATLAB and transformed back to the time domain. When combined with the transfer function from equation 12 the final solution will give the amplitude and phase response as indicated by the lock-in amplifier. The signal from the lock-in amplifier will provide the real and imaginary part of the wave response, which can easily be related to the amplitude and phase using Euler's formula. The real and imaginary parts are related by:

$$\text{Re}[H(t)] = \text{Re}[Z(\omega_o) \exp(i\omega_o t)] = A \cos(\omega_o t + \varphi) \quad (34)$$

$$\text{Im}[H(t)] = \text{Im}[Z(\omega_o) \exp(i\omega_o t)] = A \sin(\omega_o t + \varphi) \quad (35)$$

where A is the amplitude and φ is the phase as given by the solution of equation 13 and 12 in the time domain. It is important to point out that equation 13 contained the additional constant β that contained information about the thermoreflectance coefficient, energy per pulse, surface reflectivity, and detection gain, which if fitting data to a pure in-phase amplitude would be required, however in order to reduce uncertainties and simplify the fitting procedures it is common to take the ratio of the in the in-phase and out-of-phase components of the signal. In this case the β is canceled out and the solution is no longer dependent on the information contained within it. The experimental data is fit to the model using a least-square minimization routine. An example of an experimental measurement with fit data for Si can be seen in Figure 23 where V_{in} and V_{out} correspond to the measured in-phase and out-of-phase components from the lock-in amplifier respectively.

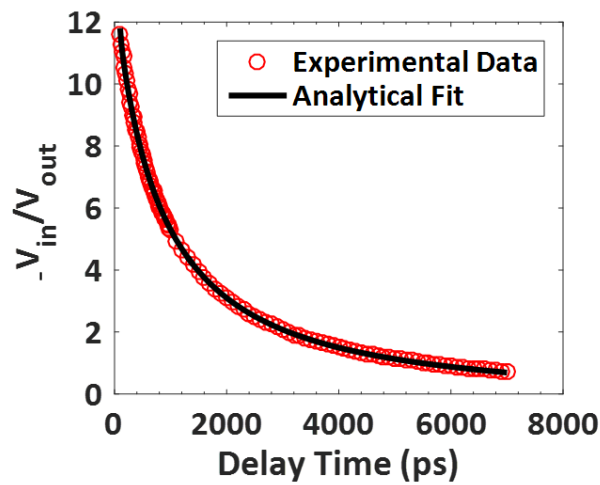


Figure 23. Measured TDTR data for a Si sample with 90nm of Al used as a transducer. The fit value for thermal conductivity was ($k=143$ W/m-K).

The analysis presented in this section should be sufficient to provide a basic idea to any graduate on the process involved in solving the heat equation for TDTR and understanding how it is then interpreted as an electronic signal read by a lock-in amplifier. This was by no means a complete and thorough analysis of all the steps and concepts involved to warrant a complete understanding of the process. There exist many great resources on the subject which can be found in the following references [122, 127, 130, 135, 137, 138, 140]

3.3.4 Measurement Sensitivity

For each layer in a TDTR model there are at least 5 parameters that must be well characterized. The in-plane and out-of-plane thermal conductivities, (κ_r and κ_z), the density, ρ , the specific heat capacity, c_p , and the thickness of the layer. Additionally, between layers there exists an interface conductance, however due to mitigating factors, this parameter is usually required to be fit in the model. As the number of layers in the model increases, it becomes significantly more important to understand which parameters will impact the accuracy of the measurement and subsequent data fitting most significantly. Variations in the chosen EOM frequencies will also impact how specific parameters impact the measurement due to variations in the thermal penetration depth. For a TDTR measurement, the sensitivity is most often defined as [135]:

$$S_\alpha = \frac{\frac{\partial R}{\partial p}}{\frac{R}{p}} = \frac{\partial R}{\partial p} \left(\frac{p}{R} \right) = \frac{\partial \ln R}{\partial \ln p} \quad (36)$$

Where R is the ratio $\frac{-V_{in}}{V_{out}}$ and p is a parameter of interest. This can be described as the fractional change in the thermorefectance signal due to a fractional change in an

independent parameter. This is essentially taking the partial derivative across the model with respect to a given parameter and normalizing the change of the slope of the solution with respect to the initial parameter value and ratio value at a given position. It is often the case that a sensitivity analysis will plot the sensitivity of parameters with respect to the delay time, but it is also equally useful to understand how the sensitivity of parameters may change with respect to both frequency and spot size [141], or the materials thickness [142]. Figure 24 gives an example a TDTR sensitivity plot for a bulk Si sample with an 83 nm Al transducer.

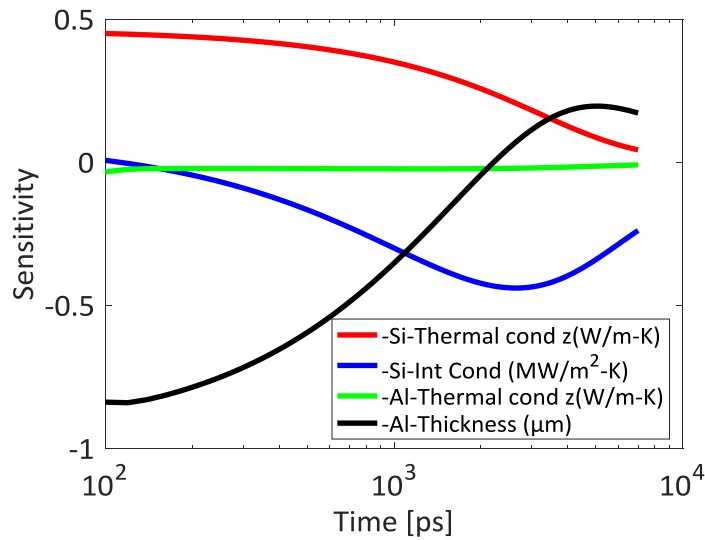


Figure 24. TDTR Sensitivity plot for a bulk Si sample with an 83 nm Al transducer.

It is assumed in Figure 24 that the Si has a thermal conductivity of 138 W/m-K, an Al/Si TBC of 155 MW/m²K and an Al thermal conductivity of 150 W/m-K. One important aspects of these types of plots is that the positive or negative value are not of great concern as they only indicate the direction of the slope change in the partial derivative. Rather it is the magnitude of the values and how they vary with time that is of interest. Because the Al

transducer is a thin film here of only 83 nm, the thermal conductivity of this layer does not have much impact on the measurement, however the sensitivity of this parameter will increase as the thickness of the transducer increases. It is important to consider this thickness and the accuracy of the thermal conductivity in the model. Typically the thermal conductivity of the Al is measured independently using electrical probes and the Wiedemann-Franz law [143].

3.3.5 *Picosecond Acoustics*

It is apparent from Figure 24 that the Al transducer thickness has a very high sensitivity to the measurement. This is almost always the case with TDTR measurements, emphasizing that an accurate measurement of this parameter is necessary in order to avoid large propagating errors into the measurement of the actual parameter of interest (usually the thermal conductivity and/or the TBC). Both atomic force microscopy (AFM) and profilometry are capable of measuring a step edge on the order of a few nanometers, however this does require that during the deposition the sample is masked in order to create the edge or scratching of the sample post metal deposition. Other methods such as ellipsometry and interferometry are not possible due to the thin film being opaque. Even if the thickness of the Al was measured at a step edge with AFM, there can often be variations in the deposition of a few nm's, which is sufficient to cause large errors in the fit value of interest.

A much more preferred method to estimate the thickness of the transducer layer is picosecond acoustics. TDTR systems are well suited to perform this measurement due to the ultrafast laser on which the system is based. TDTR is capable of picosecond temporal

resolution which allows for the ability to detect changes in the transducer's reflectivity on a scale suitable to acoustic waves. Using this method, we are able to measure the thickness of the transducer at the exact measurement location in-situ. This is because many metals are piezoreflective materials that experience a change in reflectance with strain [144]. After the laser impacts the Al film, the heating and expansion creates a strain wave in the material. The wave propagates through the material with a speed equivalent to the speed of sound in the material. Once the wave reaches the interface between the Al and the underlying material, a portion of the wave is reflected back to the surface of the Al, dependent on the acoustic impedance mismatch between the two materials [145]. Once the reflected strain wave returns to the surface it creates a brief change in the reflectivity and can be directly observed in the TDTR measurement as either a peak or valley in the measurement signal. The cleanliness of the interface can also play a significant role in the strength of the echo and can often make it difficult to pinpoint the exact time at which the echo occurred. The relationship between the propagation time and the film thickness (h_{film}) is:

$$h_{film} = \frac{v_s \tau_{echo}}{2} \quad (37)$$

where v_s is the longitudinal speed of sound in the material (6.42 nm/ps for Al) and τ_{echo} is the time it takes for the wave to propagate through the material and return to the surface as indicated in the measured demonstrated in Figure 25. The factor of two is to account for the fact that the time measured encompasses the wave passing through the material twice.

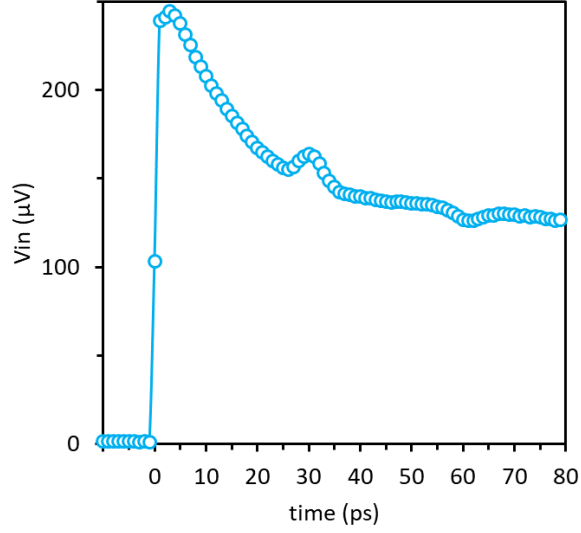


Figure 25. Picosecond acoustic sample measured with TDTR. The sample consisted of a bulk GaN substrate with 100 nm of Al as the transducer.

3.3.6 Uncertainty Estimation with Monte Carlo Method

As with all experimental procedures, understanding of the sources of uncertainty and error in the measurement are crucial to producing reliable and trusted results [117]. This is no different with TDTR and plays an extremely important role due to the significant number of parameters and often conflicting material values in literature for properties such as heat capacity and density, due to materials that have defects or quality issues [146]. The often used expression for uncertainty in a TDTR experiment is given by Wei *et al.* [147]:

$$\left(\frac{\delta_c}{C}\right)^2 = \left(R \cdot \frac{\delta_\varphi}{S_c}\right)^2 + \sum \left(\frac{S_\alpha}{S_c} \cdot \frac{\delta_\alpha}{\alpha}\right)^2 \quad (38)$$

The first term on the right-hand side takes into account uncertainty in the phase of the lock-in amplifier, with the second summation term accounting for uncertainty propagation due to the sensitivity of individual parameters in the thermal model. The left-hand side of the equation is specific to a parameter of interest, in this example it is the volumetric heat capacity, although this calculation would normally be applied to all fit parameters in the TDTR model. This method has been shown to work relatively well when the sensitivity of the parameter of interest is high compared to other modeled parameters, however it has been shown that when the sensitivity of a parameters is below 0.2, this calculation can lead to uncertainties greater than 100% [141]. While it would preferable to have samples configurations that avoid such small sensitivities, this may not always be the case. In order to address this issue, our TDTR analysis incorporates a Monte Carlo routine that can provide a statistical uncertainty and increase the accuracy for low parameters with low sensitivities. In this work, the Monte Carlo method used for uncertainty estimation samples from a randomly distributed values for each parameter within a defined uncertainty window for a given parameter. The random values are then used to fit the experimental data to the model and the values for the fit parameters are recorded. This routine is repeated up to 5000 times or until all of the fit parameters converge to their distinct values. The uncertainty of the lock-in amplifier is accounted for by taking up to 20 measurements at each delay time, generating a mean and standard deviation.

As mentioned, the Monte Carlo method requires that the user prescribe the uncertainty bound for the non-fit parameters. It then uses these bounds from which to sample random values that are used in the model fitting. For our Al transducer thickness, which typically has the largest sensitivity, we assign an uncertainty equal to 1 ps or 3.2 nm.

The thermal conductivity of the transducer is assigned a 10% uncertainty based on what has been reported in literature when using a four point probe method and the Wiedemann Franz law [148]. The pump and probe diameters are measured using a beam profiler with a reported manufacturer's uncertainty of 2%, although at small spot diameters this can increase, and the beam size becomes much more significant in the thermal model. The volumetric capacity values are taken from literature for specific samples. A thorough literature review is typically performed in order to understand variations in reported values for a material. If there is little to now variation in literature, then the material is assigned an uncertainty of only 2%. Otherwise, a standard deviation in literature values is assessed and used as the uncertainty. All parameter values with an uncertainty assigned are normally distributed and chosen at random. For our system this technique has been previously verified with Si [141]. Figure 26 shows a graphical representation of the process with corresponding normal distributions for the thermal conductivity and TBR of Si.

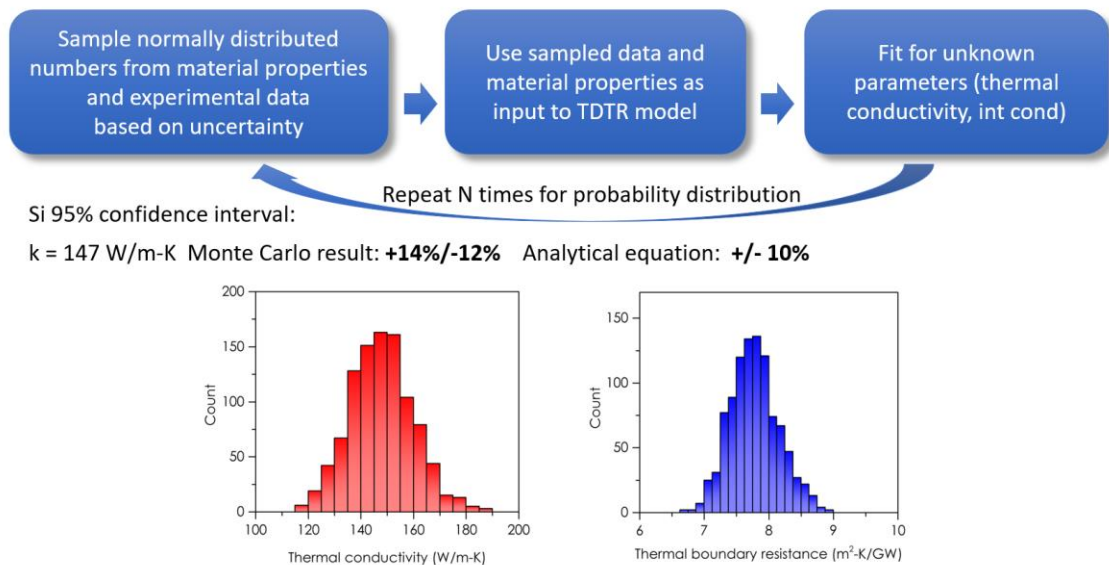


Figure 26. Representation of the Monte Carlo method as it is applied to TDTR uncertainty in this work. Adapted from [149].

CHAPTER 4. THE IMPACT OF THERMAL BOUNDARY RESISTANCE IN GAN-ON-SI EPITAXIAL LAYERS

4.1 Overview and Approach

GaN and Si are not lattice matched materials and the growth of the layers typically take place at high temperatures ($\sim 1000^\circ\text{C}$ [150]) causing the issue of the coefficient of thermal expansion mismatches ($\text{CTE}_{\text{GaN}} = 3.9 \times 10^6 \text{ }^\circ\text{C}^{-1}$ [151], $\text{CTE}_{\text{Si}} = 2.6 \times 10^6 \text{ }^\circ\text{C}^{-1}$ [152]) and creating significant strain in the GaN layer [153, 154]. This strain not only reduces the quality of the GaN through the creation of dislocations [155], but also limits the GaN layer thickness before the stored strain energy induces cracking [154]. In this scenario, intermediate layers between the GaN and Si are used in order to relax the strain in the active GaN layer, thereby reducing the defects in the GaN. The reduction of defects is directly related to the quality, performance, and reliability of the manufactured device. Selvaraj *et al.* have previously demonstrated the termination of dislocations for a GaN/Si structure with a GaN/AlN SL in comparison to an AlN only transition, as well as an increased breakdown voltage for a device built on the SL structure [156]. The ability to grow thicker epitaxial layers is an additional consequence of the interface engineering as demonstrated by the growth of $4 \text{ }\mu\text{m}$ thick GaN by Shen *et al.* [157], previous efforts without an SL structure saw reported GaN thicknesses of $\sim 1 \text{ }\mu\text{m}$ [158].

The interface engineering is accomplished by growing intermediate layers between the GaN and the Si that can consist of AlN and AlGaIn or in many cases a SL structure that will be composed of alternating layers of AlN/GaN or AlN/AlGaIn. The main reason for the strain engineering is to reduce the tensile strain in the GaN channel layer, and in many cases actually reverse the strain to a compressive state. This is because during the fabrication of the HEMT a very thin ($\sim 20\text{nm}$) AlGaIn layer is deposited onto the GaN in

order to create the two dimensional electron gas that facilitates charge transfer in the device [14]. The lattice spacing of the AlGa_N however is assumed to follow Vegard's law based on the percentage of Al content in the material, and in all cases is smaller than the Ga_N [159]. Because the AlGa_N deposition layer is substantially less than the Ga_N it is typically a valid assumption that during the deposition the AlGa_N layer takes on the same lattice constant as the Ga_N. This creates a large residual tensile strain in the AlGa_N. Under device operation, the AlGa_N will experience changes in stress due to both thermoelastic effects, and the inverse piezoelectric effect. With an already elevated residual stress state the cyclic nature of the stress becomes a concern for device reliability [65].

Not only does the reliability concern stem from enhanced cyclic stress, but the device performance, lifetime, and reliability are also directly linked to operational temperature and by extension the degree of self-heating. It is because of this that efforts to engineer the interface between the Ga_N and Si should also strive to maximize heat dissipation as well as stress relaxation.

In order to investigate how interfacial layers impact the thermal resistance and stress in a Ga_N on Si device a material system consisting of Ga_N on Si is explored using TDTR, Raman, and PL. This study examines stress related issues in the material system that in turn create a necessity to implement a specially engineered interlayer that is shown to significantly add to the thermal resistance of the material system [142]. A complete thermal and structural analysis of Ga_N that is epitaxially grown on Si is completed through evaluation of the Ga_N thermal conductivity, analysis of material strain, the effective TBR between the Ga_N and Si. Finally, the thermal device impact is evaluated with two finger HEMT devices developed with both a simple AlGa_N/Al_N transition layer and devices developed using a much more complex SL consisting of repeating layers of Al_N/Ga_N.

We used optical techniques to evaluate intrinsic material properties and device performance for a series of GaN on Si devices and wafers. In our initial work we use TDTR to measure the TBR between GaN and Si on several device stacks with increasing complexity. We began with samples consisting of an AlN or SL transition layer grown on Si, followed by measurements of GaN/AlN/Si and GaN/SL/Si structures. The residual strain in the GaN layer is evaluated using Raman spectroscopy and PL methods, then TDTR is used to evaluate the GaN/Si TBR and the thermal conductivity of the GaN. It is the purpose of this study to better understand the potential trade-off in thermal resistance that is incurred as a result of using SL structures to reduce the residual stress in the GaN channel. This is indicated graphically in Figure 27.

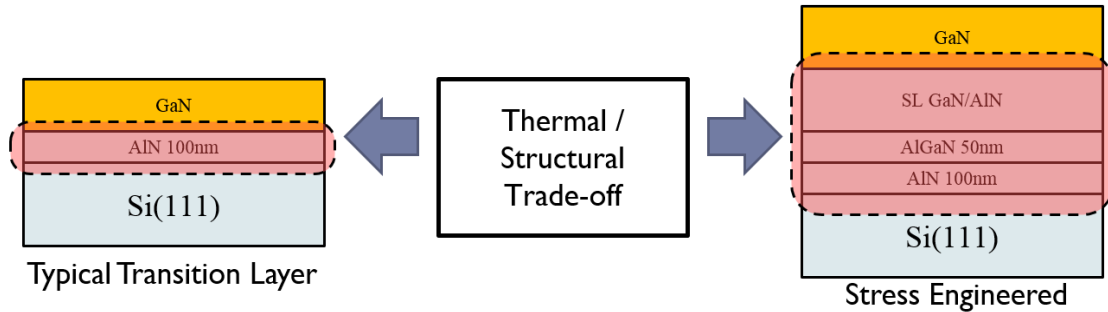


Figure 27. Example of two different transition layers used to develop GaN-on-Si HEMTs. The potential thermal and structural impact of these layers will be observed and discussed in this study.

4.1.1 Samples for Thermal/Structural Evaluation

Several wafers of varying GaN thicknesses and interface layers were provided for this study and consist of GaN and AlN layers grown on Si using metal organic chemical vapor deposition (MOCVD). GaN thicknesses of 0.31, 0.5, 0.62, 0.84, and 1.27 μm were tested for the sample with only a single AlN transition layer. Additionally, a 0.87 μm GaN layer grown atop a 0.85 μm SL consisting of 35 alternating layers of GaN (20 nm)/ AlN (4

nm) was tested. The initial transition underneath the SL consisted of a 50 nm AlGaIn grown on top of 100 nm of AlN on top of the Si substrate. A schematic of the tested structures can be seen in Figure 28. In order to help improve the accuracy of the results, two samples without GaN layers were provided to allow for measurement of the underlying material properties and help isolate the added thermal resistance due to just the GaN layer.

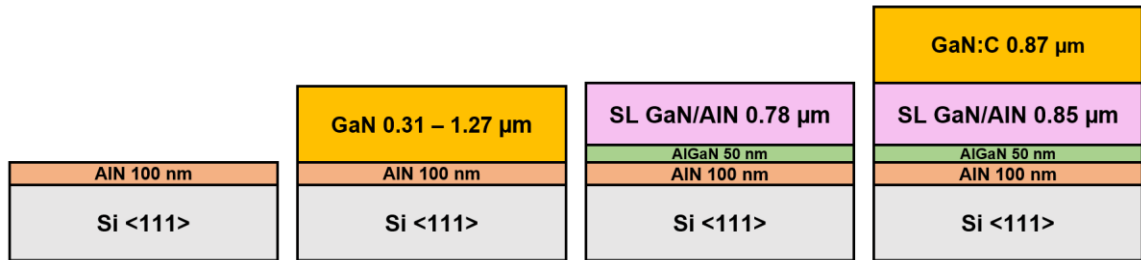


Figure 28. Schematic of samples tested in this study. The materials were epitaxially grown via MOCVD on a Si <111> substrate. The superlattice structures consist of 35 alternating layers of GaN (20 nm) and AlN (4nm). The GaN:C sample contains carbon doping on the order of $1 \times 10^{18} \text{ cm}^{-3}$.

The samples shown in Figure 28 were used to determine the GaN/Si TBR and the size dependent thermal conductivity of GaN. We were also able to determine an effective thermal conductivity of the GaN/AlN SL structure that was provided for this study. Measurements of the thickness dependent stress of the GaN were carried out with the above samples as well as the impact of the SL structure on reducing the tensile stress. Results from these studies are presented in a subsequent section. It is hypothesized that the inclusion of SL layers between the GaN and Si will increase the thermal resistance between the two materials and create a scenario where there is a higher operational temperature in HEMT devices with identical dimensions but different transition layers and by extension different residual stresses in the GaN channels. A separate set of material stacks with

HEMT devices fabricated on them were provided in order to test this hypothesis. The details of the devices are described in detail in the next section.

4.1.2 Devices to Evaluate Performance Impact

A series of six wafers, three of which contained GaN/Si transition layers composed of 100 nm AlN followed by either 550 nm or 850 nm of AlGa_N, and three of which contained SL structures composed of alternating layers of GaN/AlN that varied in thickness from 1.5 μm to 5.1 μm were provided for the device portion of this study. All the wafers contained carbon doped GaN buffer layers grown via MOCVD on top of the transition layers that were then followed by a thin unintentionally doped (UID) GaN layer to act as the device channel. The UID GaN layer was 200 nm for all devices except device E, where it was 120 nm. A schematic of the device layers with their sample letter designation (A-F) for each of the wafers is shown in Figure 29.

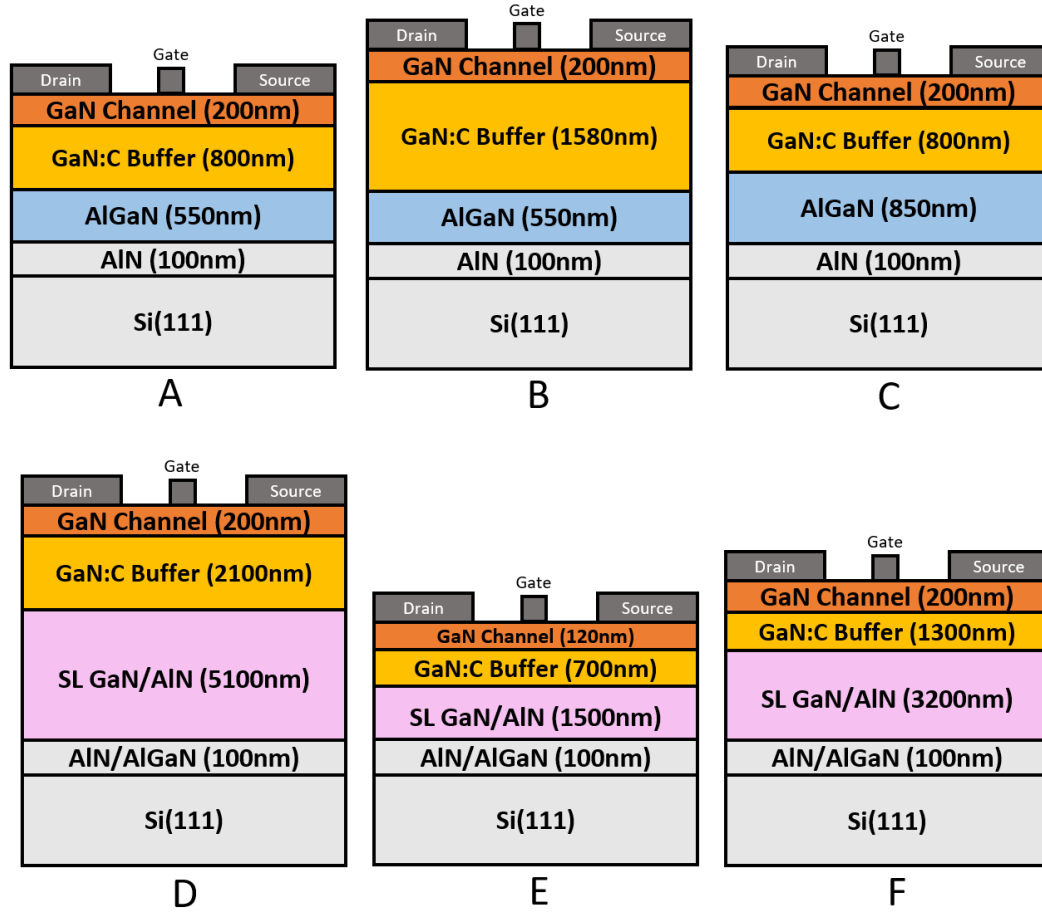


Figure 29. Cross-section schematic of HEMT devices used in this study. A-C are considered as devices with a simple transition layer, while D-F contain a much more complicated SL transition layer.

The structure of the device itself was in the form a T-shaped gate consisting of only two fingers. The devices used in this study contained no additional surface passivation. The purpose of the passivation is to suppress surface states electrically that can cause unwanted impacts during device operation by creating trapped charges between the gate and drain. This in turn depletes the 2-DEG of carriers and can limit the electrical performance by increasing the dynamic on-resistance. However, because this study is performed under a steady state condition and will only look at the thermal and structural impact of the devices, a lack of a surface passivation is actually beneficial as it allows for easier access to the

device channel using the optical methods described previously. Seen below in Figure 30 is both an optical image of the top surface of the HEMT device used in this work, along with a rendering that indicates the relevant device dimensions.

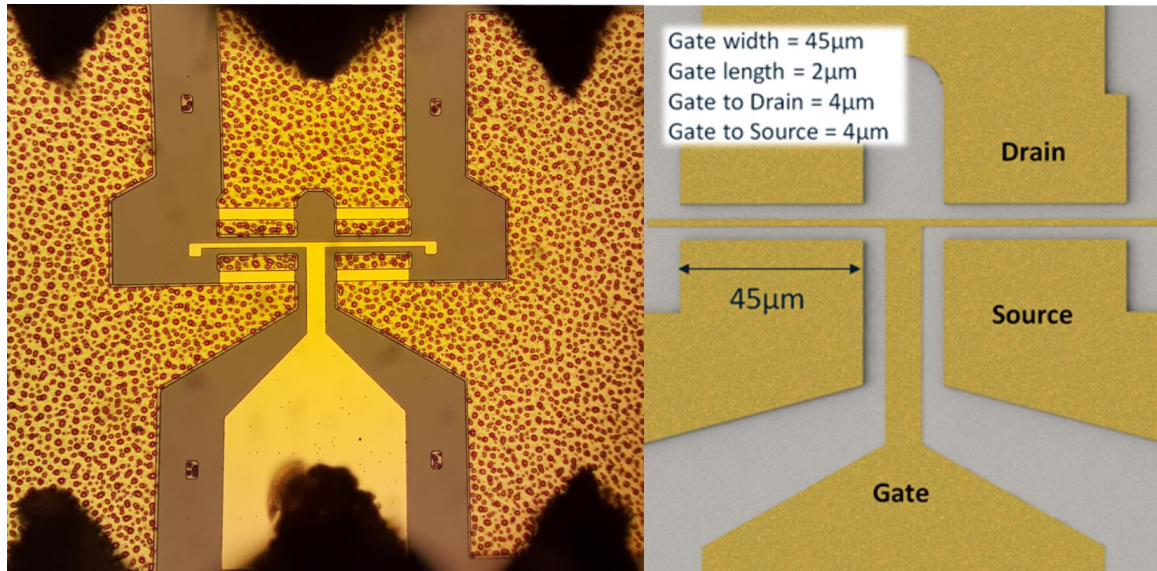


Figure 30. (Left) Optical image of the HEMT device studied in this work. The black triangles are the electrical probes that were used to power the device. (Right) A close up rendering of the gate, source, and drain region with relevant device dimensions.

4.2 Impact of Superlattice (SL) on Device Reliability

Generally, as SL is defined as a periodic array consisting of two or more materials, with the width of the materials typically on the order of nanometers. SL structures have been used extensively in semiconductor technologies since the 1970's [160]. As both the growth technologies and understanding of the quantum mechanical properties of thin films advances, SL structures have become increasingly useful for a variety of applications. They have been used to create Bragg reflectors that exploit the variations in the refractive index of the materials [161, 162]. They have been used to create quantum-well structures, resulting in unique photodetectors and solar cells [163, 164]. Significant use in LED

structures has led to advances in efficiency [165, 166]. More recently, they have been used in GaN-on-Si structures as a strain relief layer [167-169]. As mentioned, this strain relief layer is often necessary due to the significant CTE mismatch between GaN and Si. This causes the materials to expand and contract at different rates during the high temperature growth process, leading to a residual state of strain in the GaN layer. Because it is a thin film compared to a bulk Si wafer, the GaN must conform to the Si and does so stretching its bonds, leaving the material in a typically tensile state of stress. As the thickness of the GaN layer growth increase, so does the stress. Effectively this is seen and can be measured by wafer bow. If the top material has a CTE that is greater than the substrate, it will want to contract faster as the material cools and “pull” on the substrate creating concave wafer in which the valley region is the thin film. This is illustrated as a function of thin film thickness in Figure 31

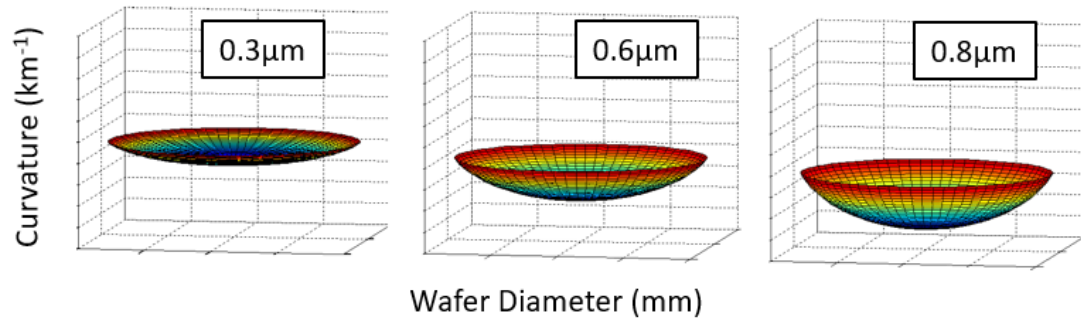


Figure 31. Illustration of how the thickness of the GaN layer impacts wafer bow.

By incorporating an AlN/GaN SL structure the residual tensile stress can be decreased or completely reversed. This is because the AlN has a CTE that is greater than the GaN [170]. This causes the GaN to contract slower than the AlN and create a situation where the material is forced to conform to the AlN layer and have a compressive strain for

the thin film. However, both materials have a larger CTE than that of Si, so it is required that several alternating layer of AlN/GaN be grown in order to compensate the tensile strain. The exact number of SL pairs that must be grown and the total thickness depend heavily on the growth conditions and the composition of the SL layers. This effect has been previously studied and found to not only change the state of stress from tensile to compressive but also resulted in a reduction of the TDD in the GaN layer [72]. This reduction in TDD is significant as it allows for both a thicker GaN layer to grow as well as a potentially higher quality GaN with better thermal properties.

4.2.1 Estimation of Stress in Device Layers

We measured the residual stress in the wafers shown in Figure 28 by using both Raman spectroscopy and PL. In the case of Raman we are measuring a through thickness average of the stress as our laser was transparent to the GaN, however with the PL measurement we are measuring the stress state near the surface, confined to ~ 80 nm. The use of PL to evaluate stress was discussed in Section 3.2.2 where we followed the procedures outlined by Choi *et al.* [113] to obtain a stress free reference and a biaxial stress coefficient for both Raman and PL measurements. The results for the structures consisting of increasing GaN thickness on an AlN interlayer along with the SL structure are shown in Figure 32. As can be seen, the stress in the GaN layer is a strong function of thickness, with the thinnest sample of $0.3\ \mu\text{m}$ resulting in a surface stress of approximately 275 ± 59 MPa. The thickest GaN sample was $1.27\ \mu\text{m}$ and found to have a surface stress state of 710 ± 110 MPa. All of the AlN transition samples showed relatively close agreement between the Raman and PL stress data, which would indicate a relatively uniform stress throughout the GaN. However, the SL transition structure displayed a significantly different trend. The

Raman through thickness measurement showed a compressive stress of 307 ± 97 MPa and a PL surface stress measurement of a tensile stress of only 8 ± 43 MPa. This is most likely due to fact that with the Raman measurement we were also sampling information on the GaN present in the SL structure. The GaN in this structure is thought to be much more compressive do to its confinement between the AlN layers. The thicker $0.84 \mu\text{m}$ GaN material is not as confined allowing it to obtain some compressive strain relief, and an almost stress-free state. It should be noted here that the yield strength of bulk GaN has been measured to be as high as 15 GPa using nano-indentation by Nowak *et al.* [171].

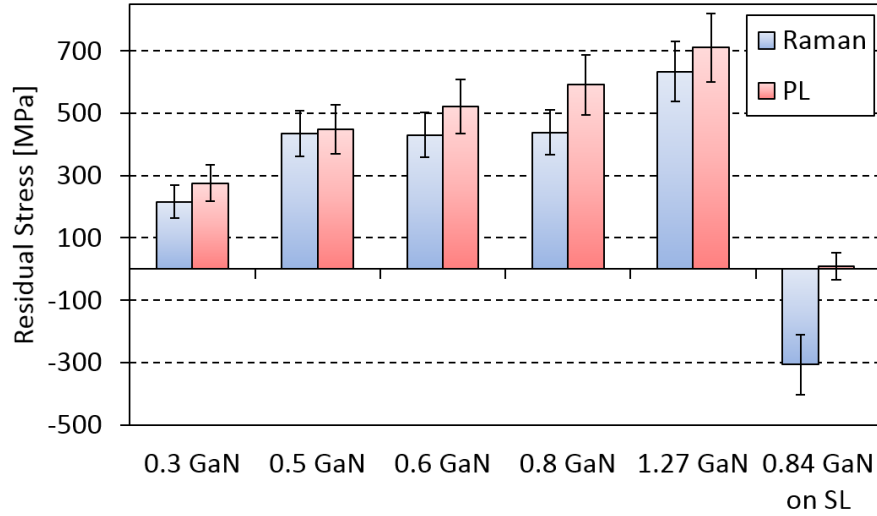


Figure 32. Raman and PL stress measurements of samples with increasing GaN thickness and one sample of GaN on a SL structure.

While the stress measured here is suitable for GaN mechanically, it is of critical importance to understand how the residual stress in the GaN impacts the stress in the very thin (~ 20 nm) AlGaIn layer that is used to form the 2-DEG. If the AlGaIn layer inside the channel were to crack, it would be detrimental for the HEMT device. To better understand this relationship, we again employed a method outlined by Choi *et al.* [113] in which the

AlGa_N layer is assumed to take on the same lattice constant as the surface of the Ga_N due to its pseudomorphic growth. We then take the measured stress and convert it to strain using the modulus of elasticity for Ga_N. This allows us to estimate the strained lattice constant of the Ga_N surface. We then use Vegard's law to interpolate a strain free lattice constant for the AlGa_N based on its composition and strain free references for both Ga_N and Al_N. We then solve for the strain in the AlGa_N under the previous assumption that the AlGa_N has taken on the same lattice as the Ga_N surface. This strain can then be converted back to stress using an interpolated biaxial modulus for AlGa_N. This procedure is shown graphically in Figure 33 with the interpreted results for the stress in the AlGa_N displayed in Figure 34. It is clear to see that the inclusion of the SL leads to a significant drop in the residual AlGa_N stress. Reduction of this stress is especially important due to factors discussed in Section 1.3. The inverse piezoelectric stress and thermal stress that is incurred during device operation happen in a cyclic manner and high levels of residual stress in the AlGa_N layer may lead to a reduced device lifetime and impact the overall device reliability. It is important to have a good understanding of all the causes of material stress in order to properly design devices for extended longevity.

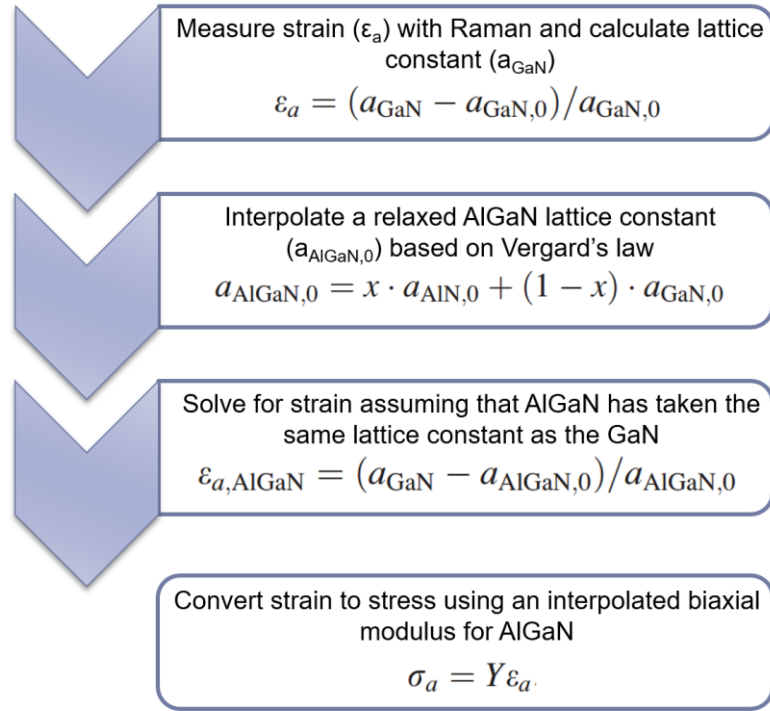


Figure 33. Graphical representation of procedure used to convert stress measured near the surface of the GaN to stress present in the AlGaIn layer. This procedure was adopted from the following reference [113].

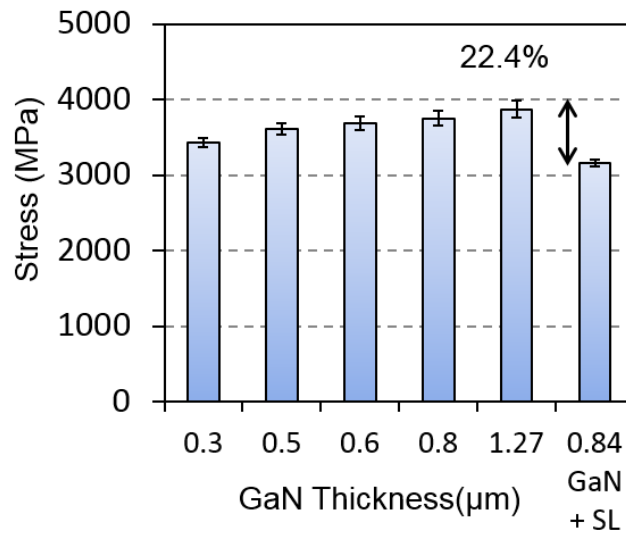


Figure 34. Estimated stress in an AlGaIn layer using the measured values from Figure 32 and the procedure outlined in Figure 33.

4.2.2 Evaluation of the GaN/Si TBR

We were unable to directly determine the thermal conductivity of the 100 nm AlN due to its lack of sensitivity in the TDTR model. However, the combined resistance of the AlN layer and the AlN-Si interface plus the interface was determined to $5.3 \pm 3.0 \text{ m}^2\text{K/GW}$. Using the Monte Carlo method described previously, we were able to determine a lower bound for the 100 nm AlN thermal conductivity as 25 W/m-K by observing the 5th percentile of the normal distribution. This is higher than many of the values reported in literature that have used MBE [172] and sputtering process [173] for AlN growth. It should be noted that previous studies have indicated a thermal conductivity as high as 47 W/m-K for a film of similar thickness based on the Born-Von-Karmen Slack model [174].

For the GaN/Si TBR measurements, consideration of the thermal resistance of the 100 nm AlN layers was included in the overall measured resistance. This means that the effective TBR consisted of three distinct thermal resistances summed together that were impossible to separate with current measurement methods. Mathematically this is shown as:

$$GaN/Si \text{ TBR} = R_{GaN-AlN} + R_{AlN} + R_{AlN-Si} \quad (39)$$

Where each component corresponds to the TBR between the GaN-AlN, the diffusive resistance due to the 100 nm AlN, and the TBR between the AlN/Si substrate respectively.

The measurements of the GaN/Si TBR were performed at a TDTR frequency of 6.3 MHz and resulted in a low sensitivity to the parameters of interest for all cases of the GaN thickness. Figure 35 shows the sensitivity of the GaN/Si TBR (shown in the figure as

$R_{\text{AlN,eff}}$), the GaN thermal conductivity, and the Al/GaN TBR (shown as $R_{\text{Al/GaN}}$). The Al/GaN TBR must always be fit for in the model because the exact deposition environment and quality of the transducer is not consistent, although since this is the most sensitive parameter in our model it contains a high accuracy. However, here we are not interested in this parameter, rather only the GaN thermal conductivity and the effective GaN/Si TBR. As seen in Figure 35, we maintain a low sensitivity to the GaN/Si TBR even when the GaN thickness is only 0.3 μm . For the thicker 1.27 μm GaN the sensitivity to the GaN/Si TBR parameter is even further reduced.

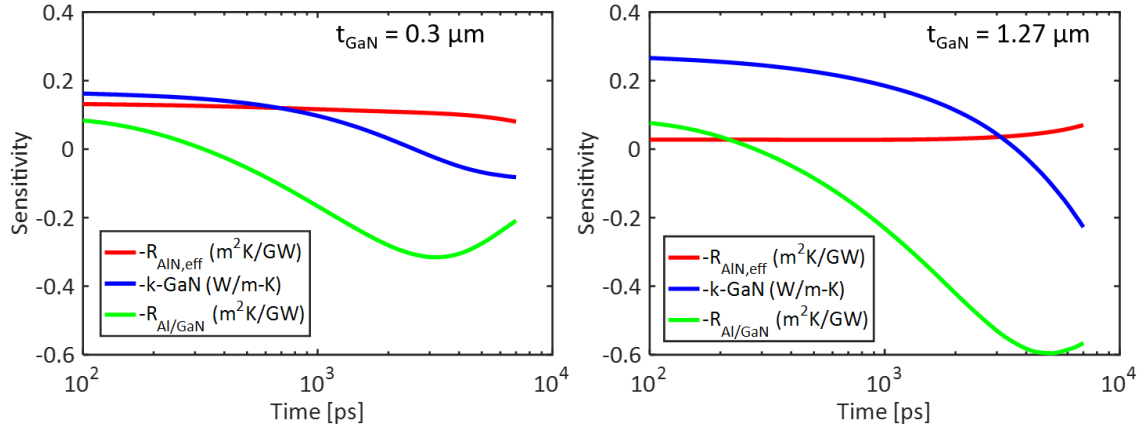


Figure 35. Sensitivity plots for the TDTR measurements of the samples shown in Figure 28. (Left) Sensitivity considering a 0.3 μm GaN thickness and (right) sensitivity considering a 1.27 μm GaN thickness.

In an attempt to mitigate the low sensitivity of the GaN/Si TBR layer of interest we performed multiple fitting iterations where each of the of the resistance parameters indicated in equation 39 were included in the thermal model and one of the parameters is held constant over a specified range. We do this for each parameter over 100 permutations and find that for the best-fit values the other parameters would shift their values to maintain a similar total resistance for the GaN/Si TBR for each permutation. Using this method, we

find that the total resistance values for the GaN/Si TBR for the AlN only transition range between $5.3 +4.2/-2.1 \text{ m}^2\text{K/GW}$ for the thickest GaN sample and $7.0 +1.8/-1.7 \text{ m}^2\text{K/GW}$ for the thinnest GaN sample. With the largest uncertainty present in the thickest GaN sample. The results for each of the GaN samples with different thicknesses is shown in Figure 36. It is interesting to observe a trend of decreasing TBR with increasing GaN thickness. This result may tie back into the increase in tensile stress of the material as simulation work has shown that there is a possible relationship between interface conductance and layer stiffness [175]. It is also possible that the phonon DOS is changing in the GaN layer as the thickness is increased as we do also observe a strong correlation between the GaN layer thickness and its thermal conductivity. This will be discussed in more detail in the next section.

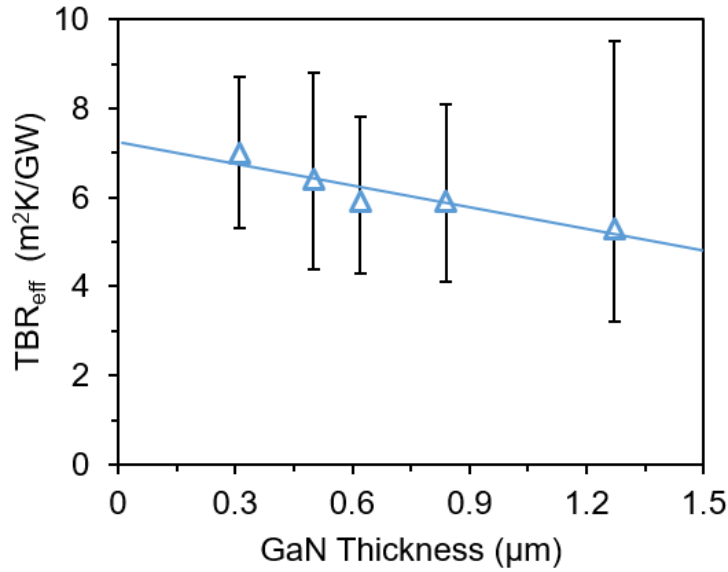


Figure 36. Effective GaN/Si TBR as measured by TDTR for each of the GaN samples consisting of only an AlN transition layer as shown in Figure 28 as a function of thickness.

Finally, the SL layer thermal resistance was estimated by measuring the thermal conductivity of the layer with TDTR. It was found to be 7.0 ± 0.7 W/m-K and exhibited a very high sensitivity to the measurement due to the relatively low thermal conductivity or high thermal resistance associated with the layer. This value is slightly lower than other SL layers measured by Koh *et al.* [176], where they found a value of 10 W/m-K for a similar SL structure. The total thickness of the SL measured in this work was 780 nm. This leads to a total thermal resistance of $112 \text{ m}^2\text{K/GW}$, which is significantly larger than the interfacial resistance measured for the GaN on AlN samples. The GaN on SL sample contained a slightly thicker SL structure than the one that was measured and would mean a larger thermal resistance of $120.4 \text{ m}^2\text{K/GW}$ as compared to a thermal resistance of $7.0 \text{ m}^2\text{K/GW}$ as measured for the $0.3 \text{ }\mu\text{m}$ GaN on AlN sample. This emphasized the thermal structural trade off, where any desire to reduce the tensile stress in the GaN through the use of an SL structure will alternatively increase the thermal resistance between the GaN and Si by a factor of 10.

4.2.3 GaN Thermal Conductivity in Devices

The thermal conductivity of GaN has been shown to vary quite significantly in literature [142, 177-180]. With a significant difference seen when considering bulk GaN as compared to thin films of only a few microns thick. In this work, we used the TDTR method to measure the thin GaN films consisting of 0.3, 0.5, 0.6, 0.84, and $1.27 \text{ }\mu\text{m}$ as shown in Figure 28. For the measurement, a good sensitivity was maintained for the GaN films above $0.6 \text{ }\mu\text{m}$, resulting in reasonable error bars. However, the thinner films all consisted of sensitivity values below 0.2. While we were still able to obtain good fits to the experimental data, this resulted in a large upper bound of error when using the Monte Carlo

method to calculate total error. We were able to establish a confident lower bound for the samples and provide a comparison to thickness dependent GaN thermal conductivity previously reported in literature by Ziade *et al.* [181]. Their sample consisted of an MBE grown GaN on SiC sample. The sample was held in the growth chamber with a molybdenum clip that slowed the growth in that region and resulted in a GaN thickness that ranged from 15-1000 nm. They used FDTR to measure along this region, resulting in measurements of the thickness dependent thermal conductivity of GaN. Our samples were grown by MOCVD which has been shown to produce slightly lower quality GaN than MBE [182], and our samples were purposefully grown to the indicated thicknesses. Figure 37 shows the size dependent GaN thermal conductivity measured in this study as compared to the values reported by Ziade *et al.*

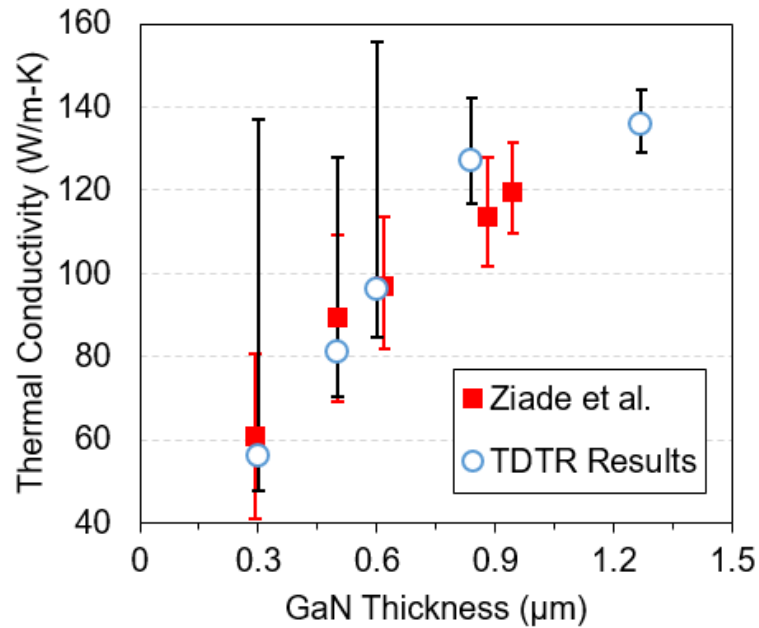


Figure 37. GaN thermal conductivity as measured by TDTR for the samples in this work as a function of the GaN layer thickness. Values measured by Ziade *et al.* are plotted for comparison.

4.3 Measurement of Device Temperatures Using Raman Thermometry

Raman thermometry is a well know method for estimating the temperature in a material based on its zone centered phonon modes. This method was briefly described in Section 3.1.2 and involves observations of how specific phonon frequencies shift as a function of temperature. When applying this method, it is crucial that the materials are property calibrated in order to develop a temperature shift coefficient that correlates with the specific material system under investigation. In this work we look at the temperature distributions of the GaN-on-Si HEMT devices described by Figure 29 and Figure 30. We were provided three wafers in which the transition layer between the GaN and Si consisted only of an AlN and AlGaN layer (samples A-C). In order to observe the thermal impacts of the SL structure, three additional samples with varying SL thickness were provided (samples D-F).

4.3.1 *TiO₂ Nanoparticles for Surface Temperature Measurements*

Raman active nanoparticles have been used previously to overcome the limitation of obtaining through thickness temperature measurements of GaN devices with silicon nanowires [183], diamond particles [184] and more recently several groups have turned to using TiO₂ and ZnO nanoparticles [185-188]. As mentioned previously, the use of a visible laser in Raman thermometry leads to a situation where the laser energy is smaller than the bandgap energy of the GaN, thereby leading to a temperature measurement that encompasses all of the GaN material. Because of the extremely localized heat in GaN HEMTs, it is desirable to understand how the surface temperature that is closer to the hotspot differs from the rest of the material. Just as important is understanding how the

interfacial layers impact the temperature distribution in the device. Here we use anatase TiO_2 nanoparticles that are distributed across the surface of the GaN HEMT devices in order to develop a through thickness temperature estimation of the device during operation. A 488 nm laser is used as the Raman excitation source. The GaN and SL structures as well as the AlN and AlGa buffer layers are all transparent to the 488 nm laser allowing it to pass through all materials where it is absorbed in the Si. A schematic of the cross-section and top view of the device with the laser source and the TiO_2 nanoparticles is shown in Figure 38.

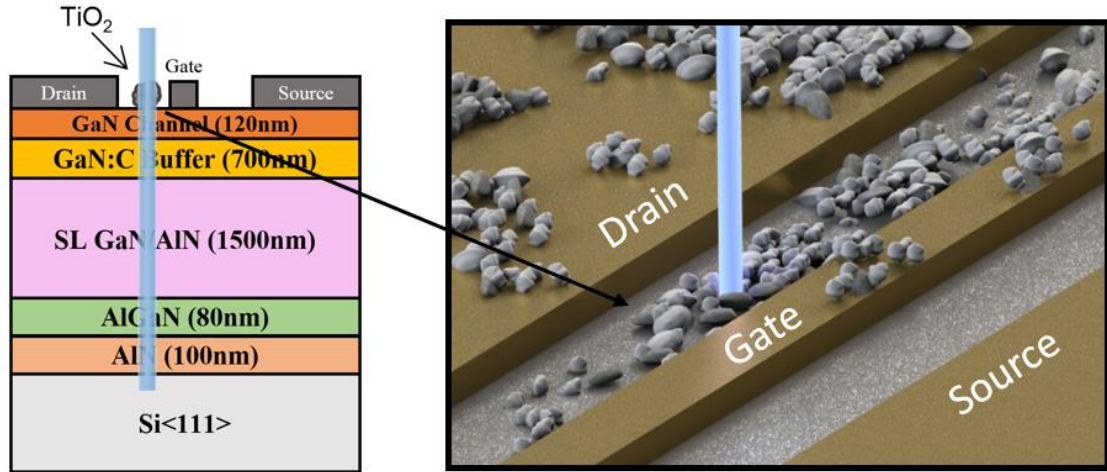


Figure 38. Schematic of the TiO_2 nanoparticle as it is positioned on the device with the 488 nm laser passing several layers and being absorbed in the Si.

When selecting a suitable nanoparticle as a Raman thermometer it is important to make sure that the material has a strong Raman active mode that is significantly separated from the active modes of the materials of interest. In this case the TiO_2 particles had a Raman shift at 143 cm^{-1} , sufficiently far enough away from the GaN $E_{2\text{high}}$ (568 cm^{-1}) and $A_1(\text{LO})$ (732 cm^{-1}) modes, however there also exists an $E_2(\text{LO})$ mode at 150 cm^{-1} that can be encompassed by the TiO_2 signal and in some cases must be accounted for with multiple

peak fitting algorithms. The samples evaluated in this did not display a strong $E_2(\text{LO})$ peak even without the TiO_2 nanoparticles. A standard normalized Raman spectra taken from sample D is shown in Figure 39. Peaks from the TiO_2 , Si, and GaN are all present in the spectra. The GaN $E_{2\text{high}}$ mode shows a double peak do to the effects of the SL structure containing highly compressive GaN as compared to that of the GaN buffer layer. For this reason the $A_1(\text{LO})$ peak was used to determine the through thickness temperature average in the GaN. All the peaks were calibrated up to a temperature of 150 °C. The TiO_2 temperature coefficient was found to be $0.0245 \pm 0.0011 \text{ cm}^{-1}/\text{K}$, Si was measured to be $-0.021 \pm 0.0001 \text{ cm}^{-1}/\text{K}$, and the GaN $A_1(\text{LO})$ coefficient was $-0.0281 \pm 0.0006 \text{ cm}^{-1}/\text{K}$. Using this information, each of the devices were powered under the same condition and the resulting temperature in the channel between the gate and drain was measured. The results of the measured temperature rise for all devices in each material system can be seen in Figure 40 and Figure 41.

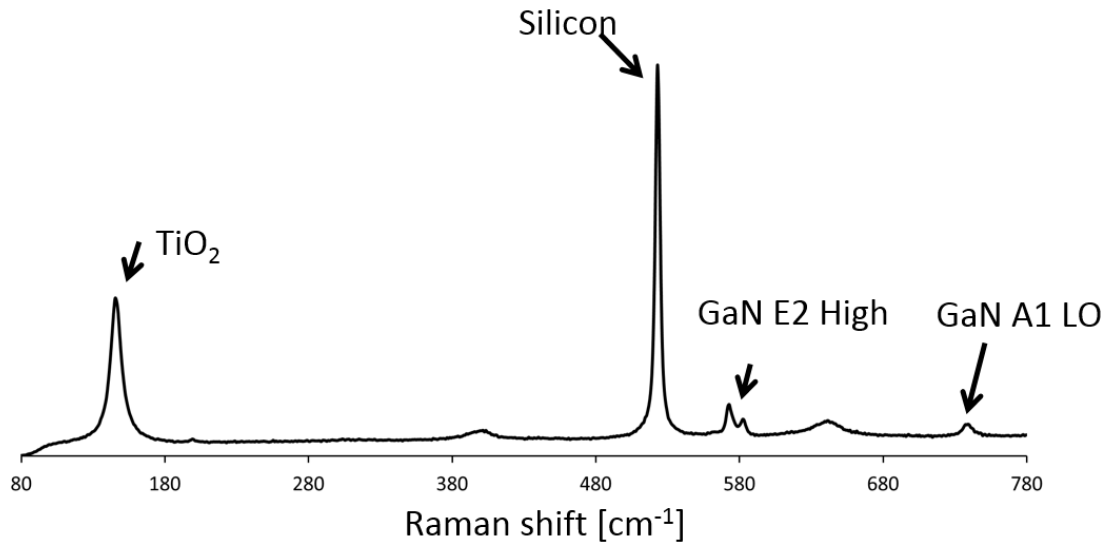


Figure 39. Raman spectra taken from sample D. It is clear to see that the GaN, Si, and TiO_2 mode are all visible.

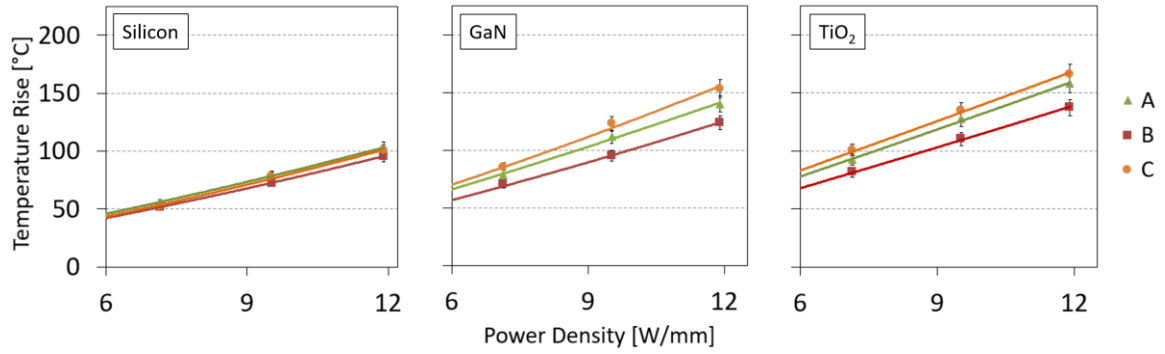


Figure 40. Measured temperature rise in the AlN/AlGaN transition layer samples for each of the Raman active materials.

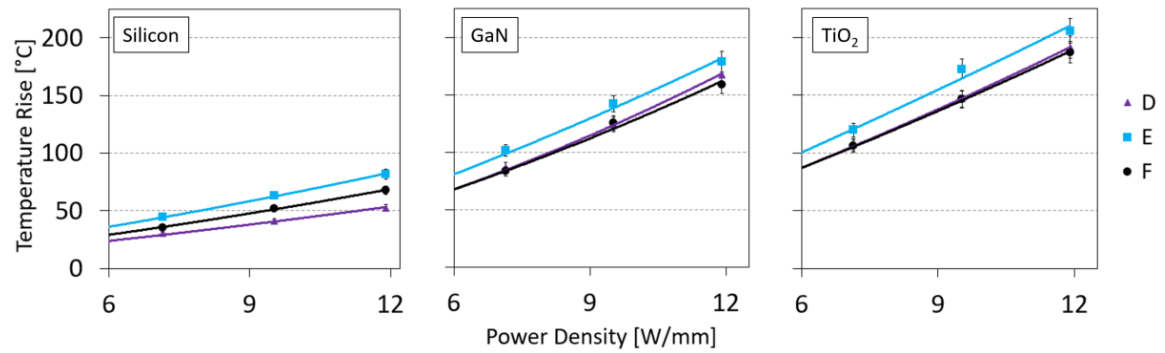


Figure 41. Measured temperature rise in the SL transition layer samples for each of the Raman active materials.

Several interesting observations can be made from the above data. For the simple AlN/AlGaN transition layer devices the temperature rise significantly less than any of the devices containing a SL transition layer. Additionally, in all cases the temperature rise measured by the TiO₂ nanoparticles is slightly higher than what is reported in the GaN material, further verifying the assumption that accurate measurement of the temperature rise in a GaN HEMT device channel requires the use of an alternative temperature sensor material when using Raman and there can be a significant temperature gradient in the GaN

material itself. If we look back at Figure 28, we can see that samples A and C are identical except for an additional 300 nm of AlGa_N present in the transition layer of sample C. This additional thermal resistance is shown due to the fact that a higher operating temperature is measured in sample C when compared to sample A. Perhaps more interesting is that sample B, while containing the same thickness of AlGa_N as sample A, had a Ga_N buffer that was almost twice as thick as sample A and yet it was shown to have the lowest temperature rise for a given power density for all of the Al_N/AlGa_N transition layer samples. This is most likely due to the thickness dependent thermal conductivity of Ga_N that was demonstrated in Figure 37. If we interpolate and extrapolate the data in Figure 37 we would find that a 800 nm Ga_N layer has a thermal conductivity close to 110 W/m-K, which is consistent with values reported by Cho *et al.*, where they measured a 0.74 and 0.85 μ m Ga_N layer to have a thermal conductivity of 105 W/m-K and 117 W/m-K, respectively [189]. On the other hand a 1.6 μ m Ga_N layer if extrapolated from Figure 37 it would have a thermal conductivity close to 160 W/m-K, consistent with a value of 167 W/m-K reported by Cho *et al.*[88]. The variation in thermal conductivity alone may be enough cause the reduce temperature in the thicker layer, but a thicker material also allows for thermal spreading to take place as the heat moves through the material towards the substrate creating a larger area for heat transfer and reducing the temperature in the device channel further.

The temperature rise of the SL samples as shown in Figure 41 all demonstrate elevated temperatures in the Ga_N material and at the surface as compared to the Al_N/AlGa_N transition layer samples. However, the temperature rise in the Si is much less for the samples containing the SL transition. This is a direct consequence of the order of

magnitude difference in thermal resistance between the SL samples and the AlN/AlGaN transition samples. As reported in the previous section the effective TBR between the GaN and Si can be as low as $5.3 \text{ m}^2\text{K/GW}$ for a simple transition layer consisting of only AlN, while at SL structure of only 870 nm accounted for a thermal resistance of $120.4 \text{ m}^2\text{K/GW}$. The large thermal resistance due to the SL layers impedes the flow of heat and is realized as a large temperature differential between the GaN and Si material. This is more easily seen if we plot all the materials in the same window and compare the two material systems side by side in Figure 42.

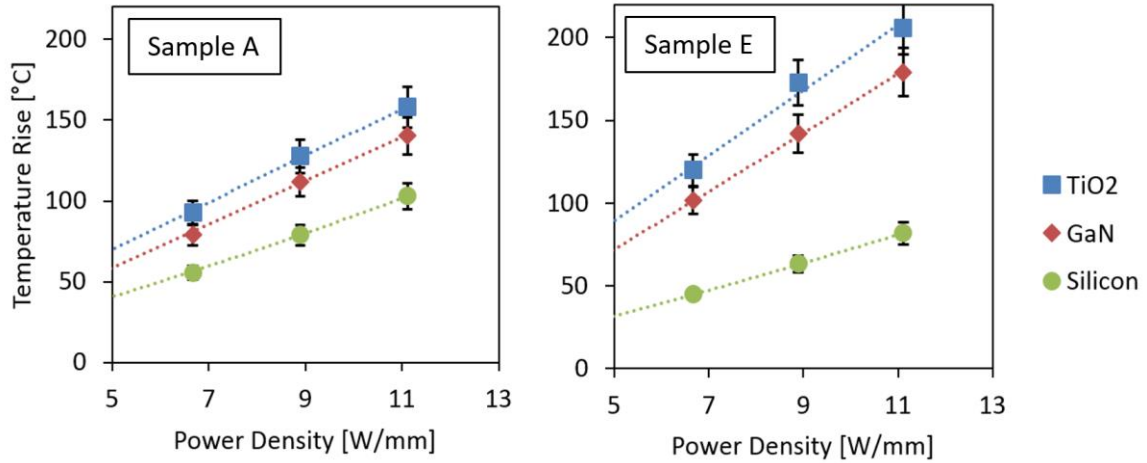


Figure 42. Comparison of the through thickness temperature distribution for a GaN HEMT device consisting of a simple AlN/AlGaN transition layer (Sample A) and an identical device with a SL transition layer (Sample E).

4.3.2 Impact of GaN Quality and Thermal Spreading Effects

Briefly mentioned in the previous section, the thickness dependent thermal conductivity of GaN can be a contributing factor to allow for devices with thicker GaN layers but identical buffer layer to operate at a lower temperature than those with a thinner GaN layer. This was shown by the reduced measured temperature in sample B as compared

to sample A even though they contained the same transition layers and sample B had a GaN buffer that was nearly twice as thick as sample A. The impact of GaN thickness leading to a higher quality and thermal spreading effects can also be seen when looking at the SL devices. Sample D in the set had the thickest SL layer of 5.1 μm , yet it was measured to have a lower operational temperature as compared to sample E with the thinnest SL layer. Again, the difference is believed to come from the quality of the GaN buffer layer. The 2.1 μm GaN buffer layer in sample D is three times that of the 700 nm GaN buffer layer in sample E. Figure 43 shows a closer comparison of the two sample measurements. There exists a 14.5 $^{\circ}\text{C}$ temperature difference in the measured surface temperature of the samples when operated at the maximum power density used in this study.

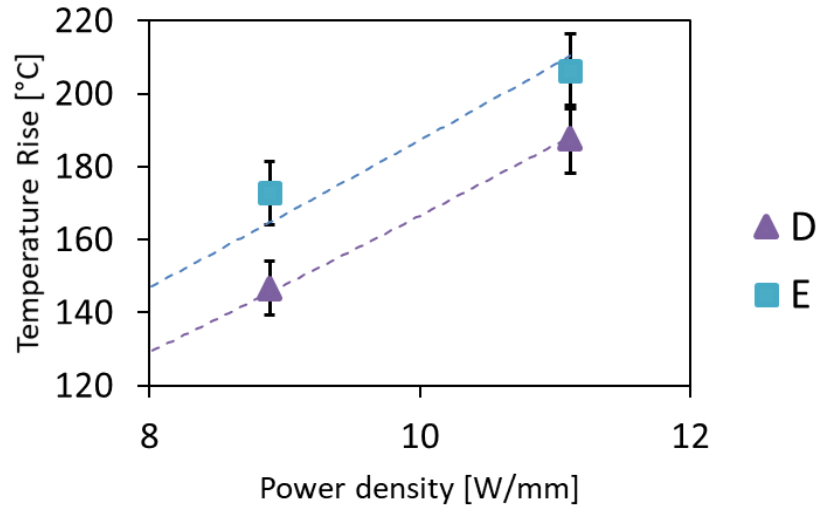


Figure 43. Temperature rise vs. power density for two samples with SL transition layers. Sample D with thicker transition and device layers demonstrated a reduced operation temperature due to an increased GaN quality and thermal spreading effects.

Further verification of the impact on thermal spreading and increased GaN thermal conductivity was carried using an FEM model with ANSYS. A quarter symmetric model

was created based on the material systems in sample D and E. Then a thermal conductivity of 200 W/m-K [184] was applied to the 2.1 μm thick GaN layer and a value of 104 W/m-K [142] was applied to the 700 nm GaN layer. Both values were consistent with what has been reported in literature. The SL layer was given a thermal conductivity of 7 W/m-K, consistent with ref. [142]. The Si was prescribed a thermal conductivity of 148 W/m-K, and the additional TBRs were not considered. The models were given a power condition equal to the largest power density used in the Raman experiments and a constant temperature condition at the base of the substrate was prescribed at 30 °C consistent with the actual experiment. Figure 44 shows the temperature rise calculated by the FEM model.

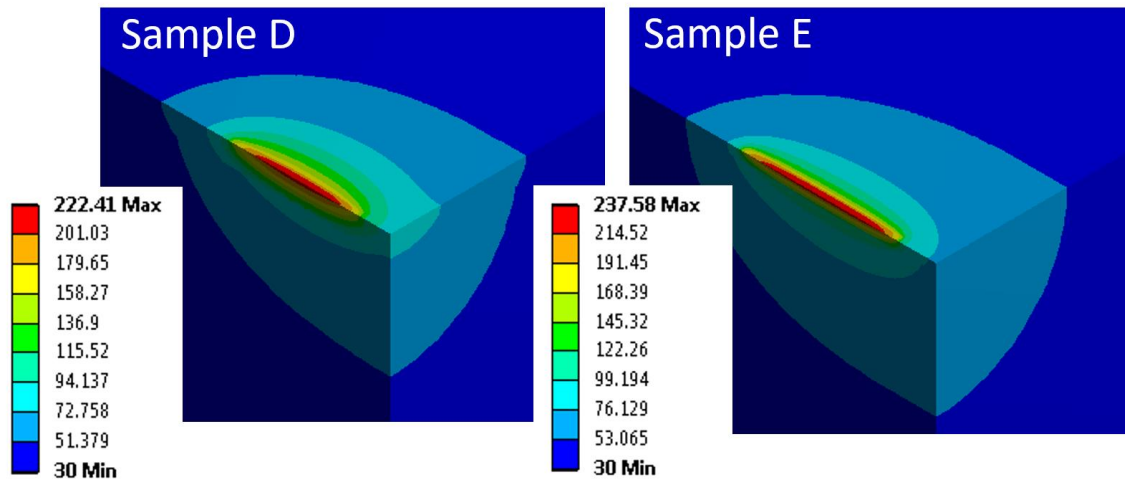


Figure 44. Temperature rise of sample D and E as calculated by an FEM model.

The impact of thermal spreading in the GaN layer can be clearly seen in sample D. The resulting temperature rises calculated by the model were 192 °C and 208 °C for sample D and E respectively. The measured temperatures for these samples was 187 °C and 206 °C for samples D and E respectively.

4.4 Conclusions

In conclusion, a complete study of a GaN-on-Si HEMT device that ties together the thermal limitations in the material by measuring the thickness dependent GaN thermal conductivity was carried out. This study clearly demonstrated how the inclusion of a SL structure impacted interfacial heat transfer and performance in a device by exploring the trade-offs between an increased GaN/Si TBR with the inclusion of a SL as a means to the residual tensile stress in the GaN. A series of HEMT devices consisting of both SL buffer layers and a much simpler AlN/AlGaIn buffer were evaluated and it was clearly shown that the size dependent GaN thermal conductivity played a role in reducing the overall operational temperature through enhanced thermal transport and heat spreading effects. The inclusion of a SL layer significantly increased the thermal resistance through the device layers as is indicated by the lower temperature measured in the Si for the SL devices when compared to the AlN/AlGaIn transition devices show in Figure 40 and Figure 41. It was shown using the non SL structures that the residual stress in the GaN scales with thickness due to GaN/Si CTE mismatch. The thermal/structural trade-off for a GaN-on-Si HEMT device was demonstrated. It was found that current architecture dictates that to have a low thermal resistance a simple (AlN/AlGaIn) interface is needed and will lead to an increased tensile stress in the GaN as compared to the SL structures. However, the ability to grow thicker GaN with the SL layer shows a higher thermal conductivity and aids in heat spreading.

CHAPTER 5. THERMAL TRANSPORT IN CVD DIAMOND FOR GAN-ON-DIAMOND

5.1 Overview and Approach

5.1.1 Thermal Transport in Diamond Films

In high power GaN transistors local power densities can approach values greater than 10 kW/cm^2 [189]. Due to the extremely high heat fluxes present during device operation, it is desirable to place a high thermal conductivity material as close to the hot-spot as possible. CVD diamond is an excellent candidate for use as a GaN HEMT substrate due to its superior thermal properties. Values of thermal conductivity ranging from ~ 700 to 2200 W/m-K have been reported for bulk CVD diamond [36]. Two popular methods for fabricating GaN-on-diamond devices consist of transferring a GaN epilayer onto a high quality CVD diamond through proprietary bonding techniques [116, 190, 191], and the direct growth of diamond on GaN, typically with a dielectric transition layer [38, 192, 193]. Sun *et al.* have shown a decrease in the effective TBR with a reduction of interlayer thickness through the use of a contactless transient thermoreflectance method and have reported values that vary from 10 to $50 \text{ m}^2\text{K/GW}$ when using a SiN dielectric layer [194].

Early work by Graebner *et al.* [195] provided great insight into the thermal properties of CVD diamond. They demonstrated the significant anisotropy in thermal conductivity that exists because of the columnar grain structure, as well as provided measurements of both thin film and bulk polycrystalline CVD diamond ranging from thicknesses of $\sim 3 \text{ }\mu\text{m}$ up to $355 \text{ }\mu\text{m}$ [196]. Building upon the interesting results from

Graebner's early work, Feldman *et al.* completed the first round robin for diamond thermal conductivity measurements in 1995 [197]. In their work, four companies supplied diamond films ranging from 300-400 μm in thickness, and measurements were performed by 10 separate laboratories. The techniques used included photothermal deflection, heated bar, laser flash, modified Ångström method, and transient grating. The samples evaluated were found to have thermal conductivities ranging from 420 W/m-K up to 1660 W/m-k. The large variations were attributed to sample non-uniformity, depth dependence of transient methods, and other unknown procedural lab variations.

A second round robin led by Graebner *et al.* was held in 1998 [196]. In this work three suppliers provided samples in which greater care was taken for consistency. The first 50 μm 's was polished from the growth surface, with the opposite surface also being polished smooth. The specimens ranged between 500-700 μm thick with thickness variation of less than 2% across the sample. There were 14 laboratories that participated, and the five techniques used were DC heated bar, modified Ångström, Mirage, laser flash, and transient thermal grating. Their resulting thermal conductivity values ranged from 1300-2000 W/m-K. Since the completion of these round robins several groups have explored CVD diamond thermal properties in more detail. Twitchen *et al.* developed a correlation of CVD diamond thermal conductivity with the IR absorption spectra of the CH_4 related defects in order to quickly determine growth quality [198]. Further studies of diamond films $> 300 \mu\text{m}$ as reported by Sukhadolau *et al.* have explored the amount of anisotropy in the thermal conductivity as less than 20 % and have looked at the relationship between methane concentration during the growth and thermal conductivity, finding significant reduction in thermal conductivity for methane concentrations $> 2 \%$ [199].

Moving forward, several groups have looked at the impact of integrating diamond in both thin films and bulk substrates into GaN devices. Cho *et al.* evaluated the impact of the TBR of bonded diamond samples to HEMT device structures through the use of picosecond TDTR and joule heating. They compared two different generations of adhesion layers and found an improvement in TBR from 108 m²K/GW to 36 m²K/GW for the first and second generation respectively [200]. The NJTT program demonstrated a 2.7x reduction in the thermal resistance of a HEMT device fabricated on a diamond substrate as compared to a GaN-on-SiC device and a 3x increase in the areal dissipation density was achieved [79]. It was found the large TBR of 47.6 m²K/GW was the significant factor in the limiting performance of the diamond device. Since this study, the impact of TBR for GaN on diamond has been studied using several optical methods and focus on the impact of the dielectric layer used to facilitate the diamond growth has been of great interest [201]. Sun *et al.* has shown that by reducing the SiN layer thickness from 50 to 41 nm a reduction in TBR from 42 to 28 m²K/GW was achieved [202]. Further work from Zhou *et al.* looked at polycrystalline diamond (PCD) used as a heat spreading material in a GaN HEMT device. By measuring the thermal properties with a transient thermorefectance approach, they incorporated the results into an FEM model to demonstrate a 12% max temperature reduction in a HEMT device with a 1 μm diamond film incorporated on top of the SiN passivation layer [203].

Recent measurements as part of the DARPA Thermal Transport in Diamond Films for Electronics Thermal Management program have demonstrated dramatic reductions in the thermal conductivity of CVD diamond near its growth interface [204]. Using TDTR, bulk diamond films and thin films of ~ 1 μm that encompassed the nucleation growth region

were evaluated, and it was found that within the thin films the diamond thermal conductivity was reduced significantly. Bulk samples demonstrated thermal conductivities up to 2200 W/m-K [36] as previously mentioned, while the thin diamond films showed a high anisotropy with $k_z \sim 180$ W/m-K and $k_r \sim 90$ W/m-K [204]. The reduction in thermal conductivity comes from the small diamond seeds (< 10 nm [205]) that are used to facilitate growth coalescing and creating columnar grain growth within the first few microns. This creates a scenario where the phonons will scatter at the grain boundaries in the radial direction. In the cross-plane direction there is an inhomogeneity in thermal conductivity attributed to the significant disorder near the growth interface [205]. As the diamond growth continues, dominant grains overcome this limitation, and high quality diamond can be achieved [36]. Increasing the heat conduction across the boundary and within the first few microns of the diamond is critical to allow for effective incorporation into high-power GaN devices. It is therefore desirable to better understand how the size and composition of the interface material and the nanostructure near the interface contribute to the overall TBR of a GaN-on-diamond interface.

5.1.2 Bulk Diamond Thermal Transport

The potential to use synthetically grown diamond with thermal and electrical properties equivalent to their natural counterparts allows for exciting opportunities for incorporation into high-power electronics. As part of an initiative to measure and understand thermal properties of bulk CVD diamond we were provided six samples from vendor V2. The samples were grown via microwave plasma enhanced CVD. Of the six samples provided, one was unpolished and had a surface roughness too large for the thermal characterization techniques utilized. Optical methods that rely on

thermoreflectance typically require a mirror like surface in order to provide sufficient signal and accurately reflect the analytical models that accompany the measurement. This requirement has been explored in detail for the TDTR method used in this work [206]. Two of the samples (B4 and B5) consisted of heavy boron doping, resulting in a significant reduction in thermal conductivity as can be seen in Figure 45. The measured range of thermal conductivities varies from 650 W/m-K up to 2200 W/m-K. While the exact growth conditions and recipes for each of the samples is not known, it has been shown that varying the methane concentration during the growth process can significantly alter the thermal and optical properties of the CVD diamond [207]. There has been direct observation and correlation of the absorption spectrum associated with the C-H bonds and the materials thermal conductivity [208]. Additionally, many other factors such as seed size, plasma power, and chamber temperature can have an impact of the quality of the diamond. Because of the coalescing nature of diamond growth, the final grain size can vary between samples, and has been shown to impact the thermal conductivity through enhanced phonon scattering at the grain boundaries [209]. The thermal conductivity suppression at the grain boundaries has been explored in greater detail by Sood *et al.* [210] by combining TDTR and electron backscattering diffraction (EBSD) and performing a detailed mapping within a designated region.

The samples provided were first measured using a laser flash diffusivity method by the vendor (Lab 3). This is a transient method that uses a laser to heat a bulk material and measures the temperature response on the backside of the sample as a function of time. As implied, it will provide a value of the thermal diffusivity of the sample and in order to convert to a thermal conductivity the volumetric heat capacity must be known. In addition

to the TDTR measurements performed in this work (Lab 1), another laboratory also measured the bulk CVD diamond samples with their TDTR system in order to provide verification (Lab 2). The results of all the measurements between all three laboratories are shown in Figure 45, where the Lab 1 results were measured by the author of this thesis.

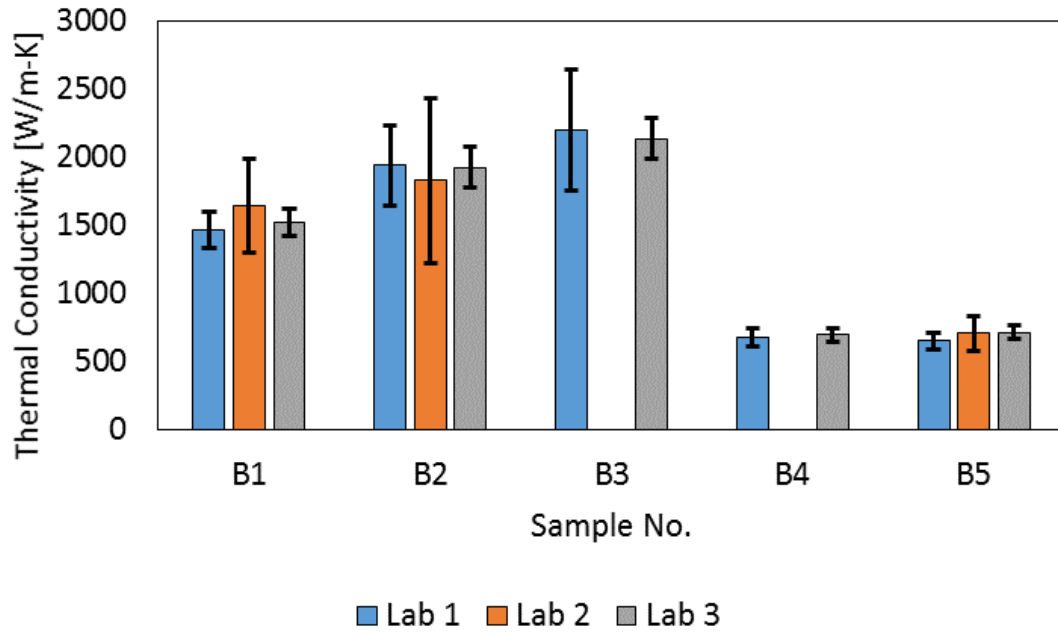


Figure 45. Comparison of TDTR and flash diffusivity results for 5 bulk CVD diamond samples measured at three different labs.

As can be seen from the results most, the different methods and laboratories were in very good agreement with little error for samples B4 and B5 that contained the heavy boron doping and a reduced thermal conductivity of 674 W/m-K and 650 W/m-K respectively. Samples B1, B2, and B3 were of significantly higher quality and the measured values were 1470 W/m-K, 1940 W/m-K, and 2200 W/m-k respectively. There was relatively good agreement between the labs and methods within the error bars, however, with TDTR it becomes increasingly difficult to accurately measure materials with high

thermal conductivities. This can be in part due to the resistance between the Al transducer and the diamond dominating the material system, thereby reducing the sensitivity to the bulk diamond layer. Other factors that can contribute to the large error and difficult come from the large increase in the TDTR in-phase signal compared to the out-of-phase signal. The ratio is very large for high thermal conductivity samples with a low thermal resistance. Because of the low out-of-phase signal the background noise inherent in the electronics can become a concern and cause significant errors in the measurement. The TDTR system used by Lab 2 was unable to measure the sample with the largest thermal conductivity due to the above signal to noise limitation. There is no measurement from Lab 2 for sample B4 due to complications when coordinating material shipments.

5.1.3 Thermal Conductivity Heterogeneity in Bulk CVD Diamond due to Grain Boundaries

For any application where diamond is used to dissipate thermal energy, an average thermal conductivity of the sample is often used in the thermal analysis to predict the impact of CVD diamond's effectiveness. However, many of the techniques that are used to measure the thermal properties of bulk CVD diamond are ineffective in measuring the local variations in thermal conductivity that can arise from the structure of the CVD diamond (local grain size, orientation, and defects). In such applications it is extremely important to understand how the underlying diamond grain structure and size impart heterogeneity in thermal properties and the subsequent impact thermal performance. This need arises when the length scales over which the thermal properties vary are on the order of or larger than the region of heat dissipation from electronic devices. The issue of inhomogeneous thermal conductivity has been discussed previously in a relatively thin film

(0.5-5.6 μm) [211]. Here however, we examine the heterogeneous thermal conductivity of bulk diamond considering local isotropic properties.

We utilized TDTR to investigate the variations in the thermal conductivity of a bulk CVD diamond sample. The sample was 13x13 mm square and 534 μm thick, heavily boron doped (10^{21}cm^{-3}), and polished on the growth side down to less than 5 nm RMS surface roughness to facilitate a mirror like finish for the TDTR measurement. The sample was mapped at several locations locally and compared to a larger sampling area that encompassed the mapped region. Measurements of the sample were performed at two different laboratories and compared to laser flash diffusivity. Additionally, characterization of grain size and orientation was provided to demonstrate the variations present in this sample and how it may relate to the local variations in the thermal properties seen in the sample.

The methodology developed to help understand local variations in the bulk diamond sample provided consists of utilizing a 5x objective to enable a pump spot diameter of 40 μm and performing several measurements at multiple areas on the sample to look at spatial variation at this scale. The sample was then kept at a single location where the 5x measurement was completed and a 20x objective was put in place without changing the sample location. It was assumed that the laser was centered within the 40 μm diameter of the 5x objective. The 20x objective allows for a spot size of approximately 10 μm . With the 20x objective we were then able to systematically map within the same 40 μm diameter that was contained within the 5x measurement. A schematic of this can be seen in Figure 46. Additionally, it was decided to perform this measurement on a sample with a reduced thermal conductivity as to reduce the signal-to-noise ratio in the TDTR

measurement and provided a higher level of sensitivity to this parameter. It was for this reason that a highly boron doped sample was chosen, rather than a similar undoped sample that has been reported of having thermal conductivities greater than 1500 W/m-K [36, 212].

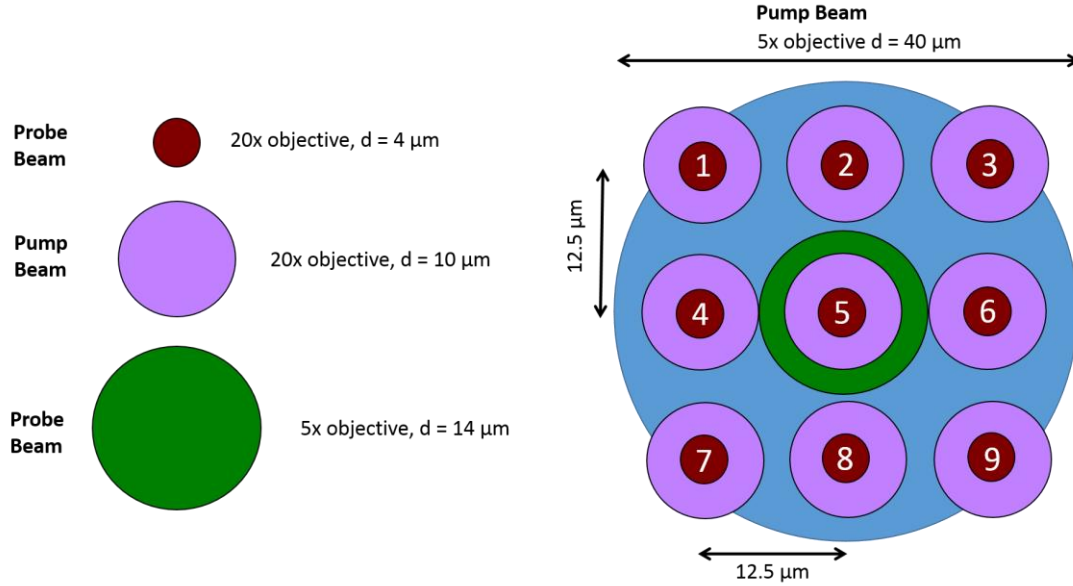


Figure 46. Schematic of representative spot sizes used throughout TDTR measurements and relative spatial locations.

In order to better understand variations in diamond thermal conductivity, the bulk CVD diamond sample studied was measured by both GT and Lab 2 as mentioned previously, however at the time of these measurements the 5x and 20x direct comparison was only performed at GT, while Lab 2 was able to provide measurements with a 20x objective and similar spot size to GT.

The measurements were performed at a modulation frequency of 3.6 MHz resulting in a thermal penetration depth of approximately 6 μm . The diamond was modeled as having an isotropic thermal conductivity for all measurements. This implies the measurement

gives an effective thermal conductivity since CVD diamond has been shown to have anisotropic thermal properties due to the columnar grain structure [211].

Results of the spatial variations on thermal conductivity when using a 5x objective at GT are shown in Table 1. Error reported in Table 1 comes from considering several possible sources of uncertainty in the measurement as well as the material itself. The significant sources of error come from our estimation of diamond heat capacity, for which we assumed a value of $1.74 \times 10^6 \text{ J/m}^3\text{-K} \pm 10\%$ [198], and the estimate of the thickness of the transducer, which is measured through a picosecond acoustic method that gives a value of $100 \pm 3 \text{ nm}$ in the case of this particular sample. In order to calculate the error in our measurement, GT uses a Monte Carlo method that has been discussed previously and reported elsewhere [142].

Table 1. Thermal conductivity variation at 4 different arbitrary locations on the diamond sample as measured at GT using TDTR with a 5x objective. This resulted in a beam size diameter of 40 μm as the sampling area. These spot numbers are not related to Figure 46.

Spot #	1	2	3	4
Thermal Conductivity with 5x obj. [W/m-K]	745 ± 77	632 ± 63	702 ± 72	687 ± 70

It is important to notice the significant variability at different measured points on the sample even with the use of a 40 μm diameter spot size; the largest variation being 113 W/m-K, which is outside the error of the measurements. Comparing these values to that of the flash measurements, we find that in all cases the reported error bars overlap. It is also important to recognize the effect the boron doping has had on reducing the thermal conductivity. Undoped CVD diamond from Lab 3 have shown thermal conductivities larger than 2000 W/m-K with the use of multiple measurement techniques [36, 212]. In

order to better understand the source of variations in our measurements we looked at two separate locations at GT and a third location at Lab 2. While efforts were made to try and ensure that both GT and Lab 2 were measuring the same locations, the lack of fiduciary marks made this a difficult task, and we report the results here as separate locations.

To investigate the thermal conductivity variations in the sample we implement the grid methodology described above where 9 smaller spot size (10 μm) measurements were completed within the larger (40 μm) spot size. The results of these measurements can be seen in Table 2. The reported error in the TDTR measurements from Table 2 is the result of variations in three or more measurements at the same spot, while the only difference comes from re-focusing for each measurement. This is important to note as the spot size of the pump beam becomes a significant source of error in the diffuse heat transfer model when using a 20x objective, and incorrect focus can result in large error.

Table 2. Results of TDTR measurements from both GT and Lab 2 for spatial mapping of a highly boron doped CVD diamond sample described in Figure 46. These results are compared to a laser flash method used by Lab 3 to determine the thermal conductivity of the bulk CVD diamond sample

Measured Thermal Conductivity [W/m-K]												
	Spot	1	2	3	4	5	6	7	8	9	20x Avg	5x (GT)
Georgia Tech	Loc. 1	817	758	554	693	740	556	701	753	526	677	687
	Loc. 2	614	605	713	616	758	750	776	650	766	700	704
Lab 2	Loc. 3	603	588	506	600	589	519	495	492	474	541	
Laser Flash	714 \pm 50											

Other interesting observations from the data show that the largest local value measured was 817 ± 71 W/m-K (GT), and the lowest measured value reported was 474 ± 11 (Lab 2). The largest variation within the 40 μm diameter was seen by GT at location 1,

spot 1 and 9, which resulted in a change in thermal conductivity of 291 W/m-K. Figure 48 shows the results of all measurements at each location. This is a 40% change in thermal conductivity in a design space that may encompass a full HEMT device, or other active electrical channels in power devices. If this change is intrinsic in the material, this could cause significant thermal issues in devices that are designed around the idea of a homogenous thermal conductivity.

Figure 47 shows a combined image of SEM and EDSB results for the bulk diamond sample reported herein. The data demonstrates that the growth of this sample had a preferred (110) grain orientation perpendicular to the plane. In this case the plan view near the growth interface was examined. Figure 49 reports the distribution of grain size in the sampled area from Figure 47.

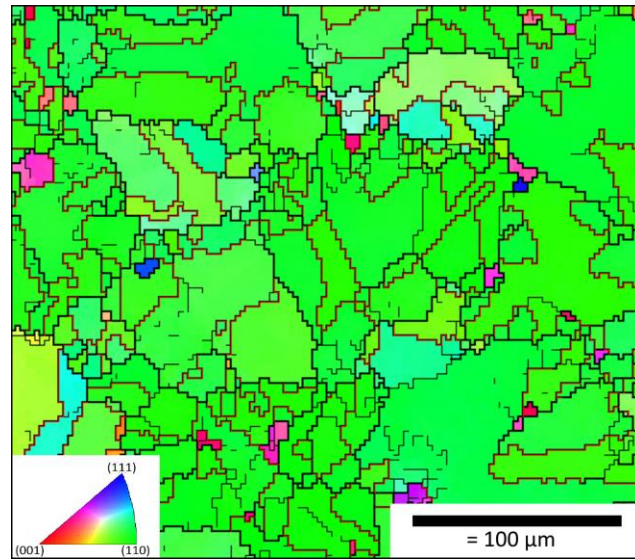


Figure 47. EBSD Orientation of sample in the normal direction shows a preferred (110) orientation. This information is overlaid with grain size analysis from SEM images.

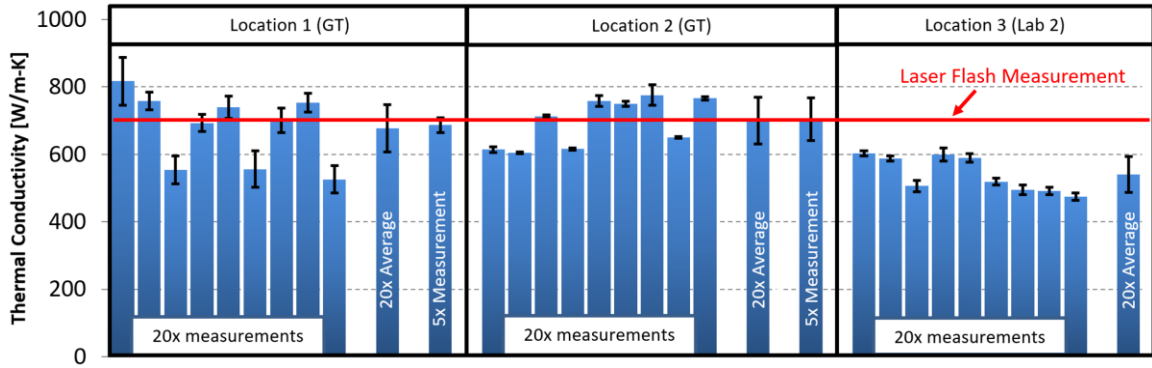


Figure 48. Data from Table 2 plotted with error bars to demonstrate the relative error for each measurement and emphasize the fact that the error bars for individual measurements seldom overlap, while the 20x averages and 5x measurements are within the designated error.

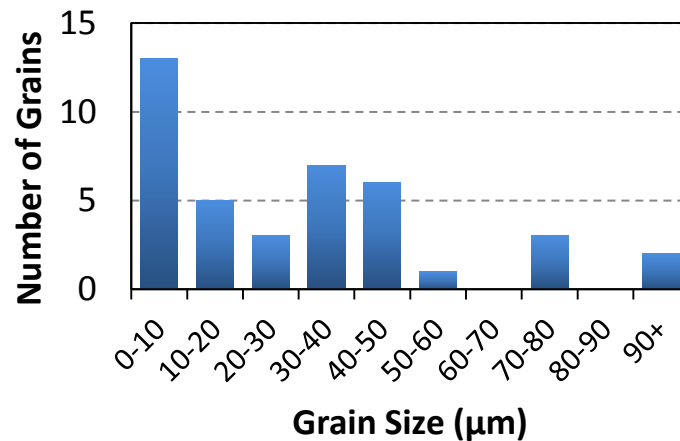


Figure 49. Relative distribution of grain size from Figure 47 shows the majority of grains in this sampled area are less than 10 μm in size.

This significant variation in grain size may be a contributing factor in the large variations in thermal conductivities that are measured in the TDTR experiments. In the case of the 20x objective the 10 μm spot size is on the order of several of the grains and could be very sensitive to being placed over grain boundaries, causing significantly reduced thermal conductivity. It is just as likely that the beam could end up in a region with a large grain and far from any boundaries, thereby measuring an elevated thermal conductivity. It

is notable that for both of the locations measured at GT the average thermal conductivity measured within the 40 μm diameter spot by the 20x objective resulted in a value very close to the 5x objective measurement as can be seen in Table 2. The TDTR data showed significant variations in thermal conductivity in the regions measured with a 20x objective, but when all nine measurements were averaged the thermal conductivity was close to that measured with the 5x objective, and the laser flash method. These data show that small spot size laser sources can be used to map the inhomogeneity in the thermal conductivity while sufficient number of grains must be sampled in order to recover the bulk effective thermal conductivity. Thus, measurements of CVD diamond with TDTR must also be accompanied by analysis of the underlying microstructure in order to have some knowledge in the heterogeneity in the underlying microstructure relative to the measurement spot size. For measuring bulk CVD diamond, thermal conductivity variations on the order of 40% can be seen over regions as small as 40 μm for grain sizes less than 10 μm . Thus, care must be taken to incorporate multiple measurements and/or large spot sizes whenever possible to account for the heterogeneous thermal conductivity between the grains.

An extension of this work was performed by Sood *et al.* [210] where they were able to create a high resolution map of thermal conductivity suppression at grain boundaries. The sample used in their work was marked with fiduciary marks in order to facilitate a direct correlation between thermal conductivity maps and grain boundaries. They were able to use a 50x objective lens with their TDTR system which resulted in a pump diameter of 4.4 μm . This allowed for the creation of high resolution maps as seen in Figure 50, which

shows a strong correlation between the measured thermal conductivity of diamond grains and the boundaries.

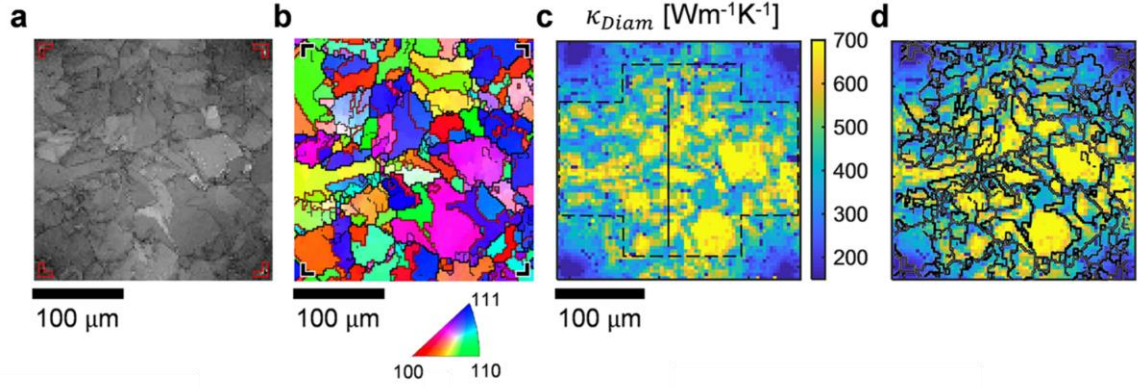


Figure 50. (a) Plan-view image of an integrated gray scale EBSD image that shows individual diamond grains. (b) In-plane EBSD grain orientation map. The color represents the crystal orientation relative to the x-axis. (c) The corresponded TDTR thermal conductivity map. (d) Thermal conductivity map overlaid with grain boundaries outlined in (b). Ref. [210]

5.2 Measurements of Vertical and Lateral Diamond Thermal Conductivity in Thin Films

The extremely large heat fluxes present in wideband gap electronic devices such as the AlGaIn/GaN HEMT along with the ever increasing maturity in CVD diamond growth as created a significant interest in potential use of thin diamond films as heat spreading layers in electronic devices. Chet *et al.* have looked at using thin diamond films in GaN LEDs as a means to spread heat [213]. Integrating thin diamond films into high power lasers components have been explored by Ichikawa *et al.* [214]. One of the most explored uses of thin diamond films has been looking at integration into high power HEMT devices [76, 194, 203, 215-218]. As mentioned throughout this thesis, the localized high heat flux requires that the thermal energy be removed from the device channel as quickly and

efficiently as possible. The potential high thermal conductivity along with its electrically insulating properties make it an excellent candidate for device incorporation. However, many studies have shown that due to the growth nature of CVD diamond the effective thermal conductivity of thin films is often significantly lower than a bulk material [36, 204]. Here we use TDTR to study the anisotropic and inhomogeneous thermal conductivity of several 1 μm and 2 μm diamond films along with a set of films ranging from 5 μm to 13.9 μm .

5.2.1 Impact of Columnar Growth on Thermal Transport

The growth of CVD diamond requires that seed crystals be placed onto the growth substrate in order to allow the gases in the chamber to nucleate onto the seeds and initiate growth. Because of this process, the diamond grows in a columnar fashion where at the growth interface significant disorder and small grains exist. As the diamond growth continues, the grains will begin to coalesce with one another to create larger grains. This leads to a situation where grain boundaries in the lateral growth direction can impede phonon transport as compared to transport in the vertical direction. This creates an anisotropic thermal conductivity in the CVD diamond. Additionally, because of the smaller grains and often even amorphous diamond found near the growth interface there exists an inhomogeneity in thermal conductivity in the vertical direction. Figure 51 shows a graphical display of the initial growth stages and the resulting grain structure.

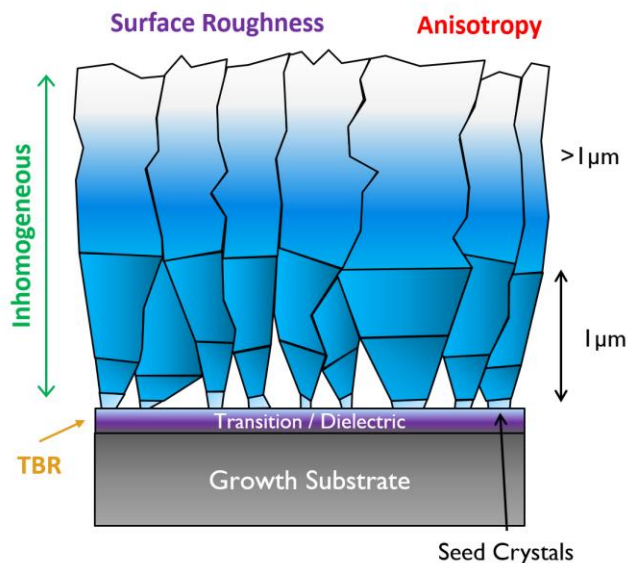


Figure 51. Graphical representation of a diamond growth demonstrating the growth from seeds leading up to a columnar structure. This leads to an anisotropic and inhomogeneous thermal conductivity. A transition layer is often used and along with the small grains at the interface can cause a large diamond/substrate TBR.

Most of the 1 μm diamond samples studied in this work were grown with a microwave power that varied between 1400-2300 W at a growth temperature of 750 $^{\circ}\text{C}$. In order to measure both the cross-plane and through-plane thermal conductivity of the diamond we used a 20x objective with the TDTR system to ensure a small spot size with a diameter of 10 μm and a low modulation frequency of 1.2 MHz. This situation is preferable to induce 2D conduction in the material. Additionally, we had specially designed samples that consisted of a 1 μm diamond film grown on top of Si that then had the backside of the Si substrate etched away. This left a suspended diamond film, which forced lateral heat transport. We were able to exploit this with TDTR to measure the in-plane thermal conductivity of the diamond films as well as measure the film on the areas where the Si substrate still existed in order to obtain cross-plane thermal conductivity values. The samples provided for TDTR measurements consisted of membrane that was a 3000 x 3000

μm square. A simple schematic of the sample is shown in Figure 52. The Al was deposited to act as the TDTR transducer. Exact measurements of the diamond thickness were provided by the growers via cross-sectional TEM to assist in the accuracy of the measurement. One of the provided TEM images can be seen in Figure 53. It is clear from the image that the interface is relatively rough and smaller diamond grains exist near the growth interface.

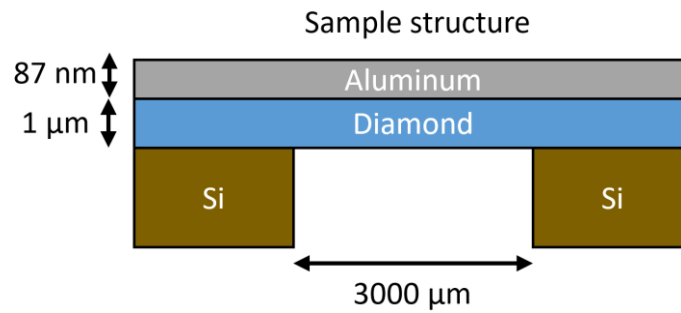


Figure 52. Cross-section schematic of suspended diamond membrane samples used by TDTR to measure both the in-plane and cross-plane thermal conductivity.

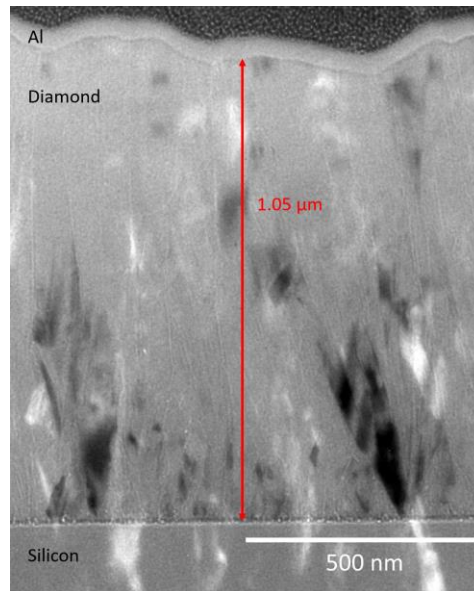


Figure 53. Cross-sectional TEM image of a CVD diamond film grown on Si.

Results of multiple 1 μm diamond sample measurements that were taken on and off the membrane are reported in Figure 54. It is evident from the data that there exists an anisotropy of about a factor of 2x, with the cross-plane thermal conductivity values slightly higher than that of pure Si. The largest recorded cross plane value for a 1 μm film in this study was 225 W/m-K. This same sample only showed an in-plane thermal conductivity of 80 W/m-K.

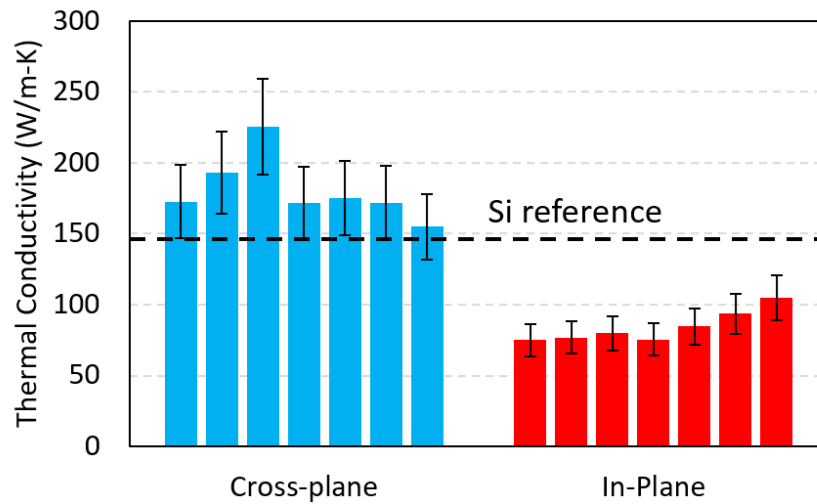
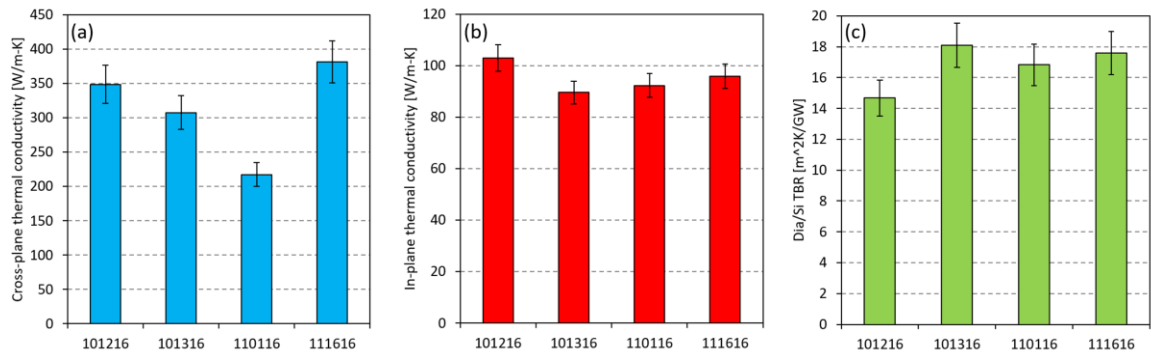


Figure 54. Cross-plane and in-plane thermal conductivity for several 1 μm thick CVD diamond films as measured by TDTR.

An additional study of several 2 μm films was performed with the intention of understanding how implementing oxygen into the initial growth process would impact thermal properties. Often O_2 is incorporated into the initial growth process as a means to eliminate or reduce the sp^2 carbon bonding. Details of the O_2 incorporation for all four of the samples measured are listed in Table 3. The subsequent measurements of cross-plane and in-plane thermal conductivity as well as the diamond/Si TBR are shown in Figure 55.

Table 3. Oxygen conditions for 2 μm diamond film growth.

Sample #	Oxygen Conditions
101216	O ₂ introduce 1 min on/1 min off during 6 min growth initiation step
101316	O ₂ introduced continuously during 6 min growth initiation step
110116	O ₂ introduced continuously during entire growth
111616	No growth initiation step; power ramped directly to 1400 W

**Figure 55.** Thermal properties of four 2 μm diamond films that were subject to differing O₂ incorporations during the growth process. (a) cross-plane thermal conductivity, (b) in-plane thermal conductivity, (c) the diamond/Si TBR for each of the samples.

From the above data there does not appear to be any direct correlation to either the in-plane thermal conductivity or the diamond/Si TBR as a function of the O₂ incorporation scheme. The in-plane thermal conductivity does not change much from a 1 μm film to a 2 μm film with both typically showing an average in-plane thermal conductivity among samples of around 90 W/m-K. However, the cross-plane thermal conductivity does increase significantly in the 2 μm samples. Additionally, the cross-plane thermal conductivities measured here appear to show a decreasing trend with O₂ incorporation, with the highest cross-plane thermal conductivity being measured on the sample that did not have any O₂ incorporated during the growth initiation.

Finally, we look a set of diamond films that range from 5 to 13.9 μm in thickness that were all grown on Si. The samples in this study were measured by both GT and Lab 2 and show good agreement within the error bounds. For these films it was not possible to measure both in-plane and cross-plane thermal conductivity, so an effective isotropic thermal conductivity is used in the TDTR model. The measured thermal conductivity vs diamond thickness is show in Figure 56.

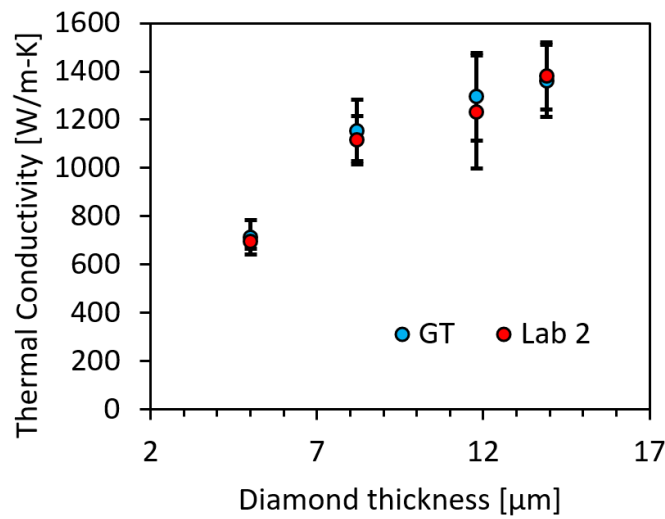


Figure 56. Diamond thermal conductivity vs thickness for films greater than 5 μm as measured by GT and Lab 2 using TDTR.

The above data shows an increase in thermal conductivity with increasing film thickness. The values range from 712 W/m-K for the 5 μm film up to 1362 W/m-K for the 13.9 μm film. For this growth recipe, Lab 3 reported the thermal conductivity of a bulk sample to be 1500 W/m-K. The rapid increase in thermal conductivity for the films < 10 μm are attributed to the grain expansion and the impact of this begins to taper off at films > 10 μm . This indicates that even with relatively thin films of ~ 10 μm , extremely high

thermal conductivity is possible and may still be a viable solution to incorporate into power devices as heat spreading layers.

5.3 Impact of Dielectric Layers on Thermal Transport at a GaN/Diamond Interface

Understanding the thermal limitations in the devices is a key challenge in creating a device that is both more powerful and reliable. The thermal pathways in an AlGaIn/GaN HEMT consist of any resistance between the active channel hot-spot formation on the gate-drain edge and the heat sink. With high-frequency devices, there is little time between switching events and placement of a highly thermally conductive material as close to the hot spot formation is extremely important in aiding in both higher power and higher frequency performance. It is primarily for this reason that silicon carbide (SiC) is used as the substrate to facilitate the heteroepitaxial growth of the HEMT device for RF applications. While much more expensive than other typically used substrates such as silicon and sapphire, it is the dominant substrate used by RF GaN industry because of the significantly higher thermal conductivity inherent in SiC ($k_{\text{SiC}} \sim 380\text{-}450 \text{ W/m-K}$, $k_{\text{Silicon}} \sim 140 \text{ W/m-K}$, and $k_{\text{Sapphire}} \sim 23 \text{ W/m-K}$). Even with an almost 3x improvement over silicon in thermal conductivity, a SiC substrate is not sufficient to fully exploit the potential of GaN. Because of this, much interest has gone into development of GaN-on-diamond technology.

Thermally speaking, the most significant bottleneck for heat transfer in a GaN-on-diamond device is encountered at the interface of the two materials. Two popular methods for fabricating GaN-on-diamond devices consist of transferring a GaN epilayer onto a high quality CVD diamond through proprietary bonding techniques[116, 190, 191], and the direct growth of diamond on GaN, typically with a dielectric transition layer[38, 192, 193].

Sun *et al.* have shown a decrease in the effective TBR with a reduction of interlayer thickness through the use of a contactless transient thermoreflectance method and have reported values that vary from 10 to 50 m²K/GW when using a SiN dielectric layer [194]. It is therefore desirable to better understand how the size and composition of the interface material contribute to the overall TBR of a GaN-on-diamond interface.

5.3.1 *Measurements of Effective GaN/Diamond TBR using TDTR*

We utilized TDTR to study the TBR of three different GaN-on-diamond interfaces. The interfaces of interest consisted of diamond-on-GaN grown with a nominal 5 nm SiN interfacial layer, a nominal 5 nm AlN interfacial layer, and a diamond-on-GaN grown with no interfacial layer. These samples were all prepared in a similar fashion, to be discussed in more detail, and henceforth will be referred to as samples S, A, and G respectively. The purpose of this study was to better understand how interfacial layers and structure design play a significant role in enhancing thermal transport in GaN-on-diamond devices through a decrease in the TBR at the interface.

The samples used in this study were all grown using a microwave plasma CVD system at Fraunhofer USA Center for Coatings and Diamond. The seeding of the diamond was carried out prior to the actual CVD diamond growth. During the diamond growth, all three samples were loaded into the reactor at the same time to ensure consistency among the samples. The growth of the diamond took place on three separate structures, one with a thin nominal 5 nm SiN interfacial layer, another with a nominal 5 nm AlN interfacial layer, and lastly a sample with no interfacial layer. These structures were grown on a 4H-SiC wafer with a 20 nm AlN nucleation layer and a nominal 500 nm GaN layer. Details for

each of the structures can be seen in Figure 57. For all cases, the diamond growth on the GaN was successful despite the differing interfacial conditions.

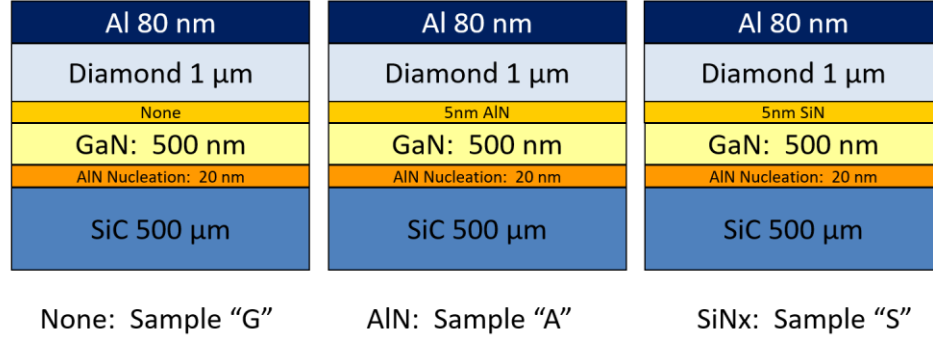


Figure 57. Sample structures used to investigate the dielectric impact on TBR for GaN-on-diamond with nominal thickness values. All samples had an additional 80 nm aluminum transducer layer deposited onto the surface of the diamond to facilitate the measurements.

The TDTR technique has proven to reliably estimate thermal properties in bulk material samples as well as thin films. However multiple thin films have proven to be quite challenging when attempting to extract thermal properties of any of the materials of interest [219]. In our case, we have a five-layer model consisting of the Al transducer, diamond, GaN, AlN, and the SiC substrate (the diamond/GaN interlayers are treated only as interface resistances). In total this leaves us with eight unknowns in our model: the Al/diamond TBR, diamond thermal conductivity, diamond/GaN TBR, GaN thermal conductivity, GaN/AlN TBR, AlN thermal conductivity, AlN/SiC TBR, and the SiC thermal conductivity. In the case of the AlN layer we treat this layer along with its respective interfaces as a combined resistive interface between the GaN and SiC. For all the layers, the heat capacities are taken from the following references [220-223] and values are displayed in Table 4. The thickness of the Al transducer layer was determined using an in-situ picosecond acoustic technique that was previously discussed and has been well documented and verified for

use in TDTR measurements [145], and the thermal conductivity of the Al was estimated by measuring the electrical conductivity of the film and applying the Wiedemann-Franz law.

Table 4. Parameters used in model fitting to experimental data for Sample S.

	k_{\perp} [W/m-K]	k_{\parallel} [W/m-k]	ρc_p [MJ/m ³ K]	d [nm]	G [MW/m ² K]
SiC	423 +16/-24*	iso	2.13 ± 0.10	semi-inf	219 +101/-40*
GaN	95 ± 28	iso	2.64 ± 0.13	580 ± 29	fit
Diamond	fit	92 ± 8	1.82 ± 0.18	1050 ± 150	fit
Al	175	iso	2.43 ± 0.12	80 ± 2	
Pump Radius [μm]	Probe Radius [μm]				
20.1 ± 0.50	7.1 ± 0.18				

* values obtained from data fitting of non-diamond samples with corresponding MC error based on 1000 iterations

Because of the relatively high thermal conductivity found in the underlying layers of diamond on GaN samples, it becomes increasingly challenging to distinguish whether the thermal resistance inherent in the material stacks emanates from the GaN-diamond interface or the GaN layer itself. To mitigate this uncertainty, we considered for comparison an additional material stack in which the diamond growth had not yet taken place, leaving simply the 500 nm GaN layer, 20 nm AlN nucleation layer, and the 4H-SiC substrate. Because TDTR is a pulsed transient heating technique, one can change the modulation frequency to obtain differing thermal penetration depths [224]. The idea of using multiple frequencies to gain sensitivity to certain parameters has been widely used in the TDTR community [135], and in this case, we are able to use a low modulation

frequency of 1.2 MHz to increase our sensitivity to the underlying substrate of SiC and the GaN/SiC TBC. For this sample we were unable to fit for the thermal conductivity of the GaN directly due to a high thermally resistive interface between the Al/GaN. Using this sample, we were able to fit the thermal conductivity of the SiC and the TBC between the GaN and SiC, and then used the fit values in the model solution for samples S, A, and G. The fit value for the SiC thermal conductivity was found to be $423 +16/-24$ W/m-K. This is an effective root mean squared value of thermal conductivity since SiC has been demonstrated to have a directional dependent anisotropy to its thermal conductivity [225]. Our measured value agrees well with what has been reported by Su *et al.* [225] using a three-omega technique, and a value of 420 W/m-K used by Sarua *et al.* [87] when matching thermal simulations to experimental Raman thermography measurements. The TBC between the GaN/SiC including the 20 nm AlN interlayer was measured to be $219 +101/-40$ MW/m²-K and agrees well with a value of 225 ± 55 MW/m²-K recently reported by Ziade *et al.* [181].

Our final model includes the diamond layer that was used along with the experimental data to fit for the Al/diamond TBC, cross-plane thermal conductivity of the diamond, and the main parameter of interest, the diamond/GaN TBC. Table 4 displays the parameter values that were used in the final model of sample S. For samples A and G the thickness of the GaN and the diamond were changed based on results of the SEM/TEM imaging (discussed in Section 5.4.2). The corresponding GaN thermal conductivity was taken from Ziade *et al.* [181] for a similar GaN/SiC interface and GaN thickness. The thermal conductivity of GaN used in the model (95 W/m-K) is lower than some of the previously published values for bulk GaN, which depending on the growth method have

been shown to be up to 230 W/m-K [226]. Additionally, a previous TDTR study of similar GaN/AlN/SiC samples has been carried out in which the thermal conductivity of GaN was reported to be 167 W/m-K for a 0.9 μm sample[88]. In their work however, the thermal conductivity is estimated by fitting three separate GaN thicknesses, 0.6, 0.9, and 1.6 μm , and assuming thickness independent properties, the slope of a thermal resistance vs. thickness curve is used to extract both GaN thermal conductivity and an effective resistance of the GaN/SiC that includes the AlN contribution. Efforts by Freedman *et al.* have used FDTR to estimate a thermal conductivity accumulation as a function of phonon mean free path (MFP)[227]. In their work they demonstrate that phonons with a MFP of 500 nm or less only contribute to about 40% of the bulk conductivity. They consider a bulk GaN thermal conductivity of 220 W/m-K, which would estimate a 500 nm thick GaN thermal conductivity to be 88 W/m-K. More recent efforts to understand the thickness dependent thermal conductivity of GaN have been undertaken by Beechem *et al.*[180], in which TDTR was used at both Sandia National Laboratories and the University of Virginia to measure 3-4 μm thick MOCVD GaN grown on an HVPE GaN substrate with differing levels of both n and p-type doping. The measured data was applied to a modified Callaway model in order to determine how the thermal conductivity changes as a function of thickness, dislocation density, and impurity concentration. In their work they find a GaN thickness of 500 nm should correlate to a thermal conductivity of ~ 100 W/m-K. As mentioned, the value of GaN thermal conductivity used in this work was taken from Ziade *et al.*[181], and agrees well with both of the previously mentioned studies.

A modulation frequency of 3.6 MHz was used during the experimental acquisition and was kept consistent among all diamond samples. The in-plane thermal conductivity of

the diamond was taken from the following reference [204], however because of the large spot size used in the experimental acquisition, there is little sensitivity to this parameter in the fit model. Results of the experiments are shown in Figure 58. For sample G (no interlayer) the TBR was found to be $41.4 \pm 14.0/-12.3 \text{ m}^2\text{K/GW}$ with some spot to spot variation. Samples A and S demonstrated a much lower spot to spot variation, and multiple measurements resulted in fit values of $18.2 \pm 1.5/-3.6 \text{ m}^2\text{K/GW}$ and $9.5 \pm 3.8/-1.7 \text{ m}^2\text{K/GW}$, respectively. Sample S with the 5 nm SiN interlayer demonstrated the lowest TBR of the three samples.

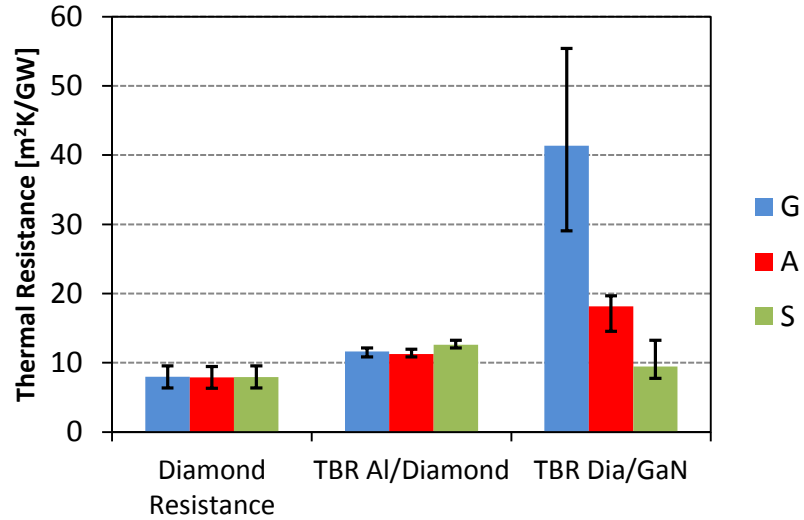


Figure 58. Measured thermal resistance of each of the fit parameters in the TDTR model.

It should be noted that a similar study was carried out on GaN-on-diamond samples that were analyzed by Gu *et al.* using a non-contact transient reflectance method that is matched to FEM simulations [228, 229]. In their analysis, they found a similar trend, albeit different values on samples with different architectures. For the sample G configuration, they report values ranging from 65-85 $\text{m}^2\text{K/GW}$, sample A has reported values from 10-18

$\text{m}^2\text{K/GW}$, and sample S has values reported between 2.5-6.2 $\text{m}^2\text{K/GW}$. While the trend is similar, it is difficult to directly compare the values with results presented here due to several key parameters such as diamond thickness that are not specified. A more recent publication by Zhou *et al.* [230] used the same transient reflectance technique as Gu *et al.* [228] and utilized samples very similar to this work. The results obtained by Zhou *et al.* are consistent with those found in this work and demonstrate the importance in better understanding the role dielectric layers used to facilitate direct growth of diamond on GaN have in contributing to the TBR of the interface. For the results acquired in this study, error analysis was carried out using a Monte Carlo technique in which all the model parameters are assigned an uncertainty (displayed in Table 4), and the parameter values are randomly varied according the specified uncertainty, then the experimental data is fit to the new model. This is performed 1000 times and a normal distribution is acquired. For our reported values, we take the 50th percentile, and error bars are acquired using the 10th and 90th percentile of the normal distribution. This method for error analysis was previously discussed and has been documented extensively in the following reference [142]. Results for the three samples are displayed in Table 5.

Table 5. Results of fit parameters for Samples G, A, and S. k was held constant according to reference [204]. Diamond thickness (d) was acquired from TEM imaging. κ_{\perp} and TBR are fit parameters.

Sample	κ_{\perp} [W/m-K]	κ_{\parallel} [W/m-k]	d [μm]	Diamond/GaN TBR [$\text{m}^2\text{K/GW}$]
G	126 +25/-22	92 ± 8	1.0 ± 0.14	41.4 +14.0/-12.3
A	159 +36/-32	92 ± 8	1.2 ± 0.11	18.2 +1.5/-3.6
S	132 +22/-21	92 ± 8	1.0 ± 0.15	9.5 +3.8/-1.7

5.3.2 Evaluation of interfaces using TEM/SEM Imaging

Sample imaging via cross-sectional SEM using focused ion beam milling (FIB) took place with a FEI Helios Nanolab 400 DualBeam system that includes an energy-dispersive X-ray spectrometer. This system is capable of resolving features on the order of ~ 1 nm. Further cross-sectional characterization was accomplished with TEM by FIB milling with a final polishing done using an ion beam accelerating voltage of 2 kV.

To better explain the differences seen in the TDTR experimental results, SEM and TEM imaging was carried out. The results of these experiments demonstrated drastic differences at each of the interfaces. For the sample with no interfacial layer between the diamond and GaN, sample G, it was apparent that there was extensive deterioration in the form of voids measuring approximately 50 nm or more at the diamond/GaN interface (Figure 59). The void formation at the interface due to etching of the GaN during the nucleation was most likely caused by a growth environment containing hydrogen (H_2) at elevated temperatures. The effect of H_2 etching in GaN has been studied in detail by Yeh *et al.*[231], and demonstrated specifically for GaN-on-diamond as a consequence of the

diamond seeding conditions by Lui *et al* [232]. In the case of sample A, bright field STEM images indicated that the thickness of the GaN was between 252 and 318 nm, and the first 30 nm appeared to be significantly roughened. Further investigation of electron energy loss spectroscopy (EELS) scanning in the region between the GaN and diamond found no evidence of Al from the AlN adhesion layer in the area with a reduced GaN thickness. However, this sample showed the formation of mesa structures at the GaN/diamond interface. It was determined that the AlN layer was deposited as a non-continuous layer and etching of the GaN occurred in areas where no AlN was present.

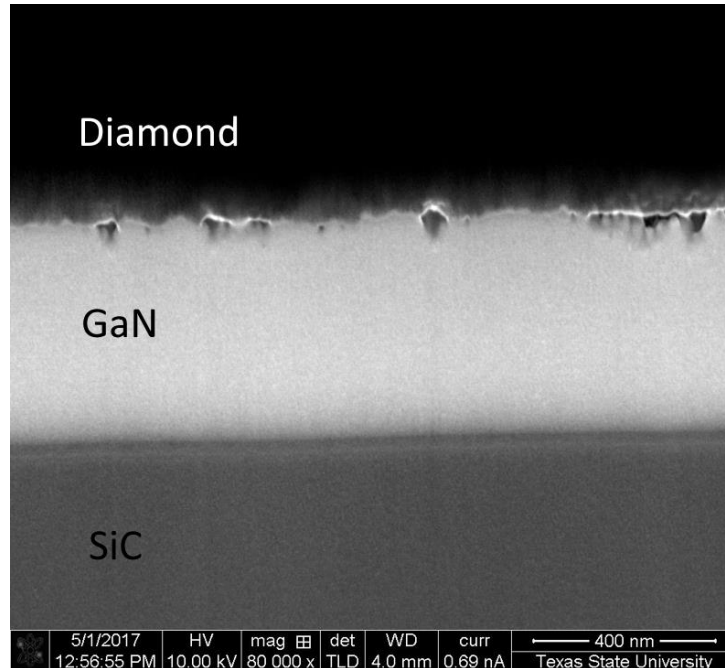


Figure 59. SEM image of sample G showing voids present at the diamond/GaN interface.

This is apparent in Figure 60b from the much smoother interface on the top of the mesa structure compared to that of the etched region, as well as the inclusion of voids in this region. In this scenario the AlN is acting as an etch barrier, but because the AlN layer is non-continuous, the harsh diamond growth environment etches the exposed GaN similar

to sample G in GaN areas not covered by the AlN. This creates a significantly roughened surface. Even though there was significant etching of the GaN, the diamond and GaN appeared to remain in intimate contact in the observed areas Figure 60a, as there were no obvious signs of delamination of the diamond layer. Additional low voltage darkfield STEM did reveal small voids at the diamond/GaN interface as seen in Figure 60b. This sample did demonstrate a lower TBR compared to sample G (Figure 59), due to the smooth interfaces where the AlN was present, and the better adhesion of the diamond film. The TDTR measurement utilized a spot size with a 40 μm diameter, so it is likely that the measurement area encompassed both regions of the interface. This is further verified by observing the plan view SEM of sample A before the diamond deposition as shown in Figure 61.

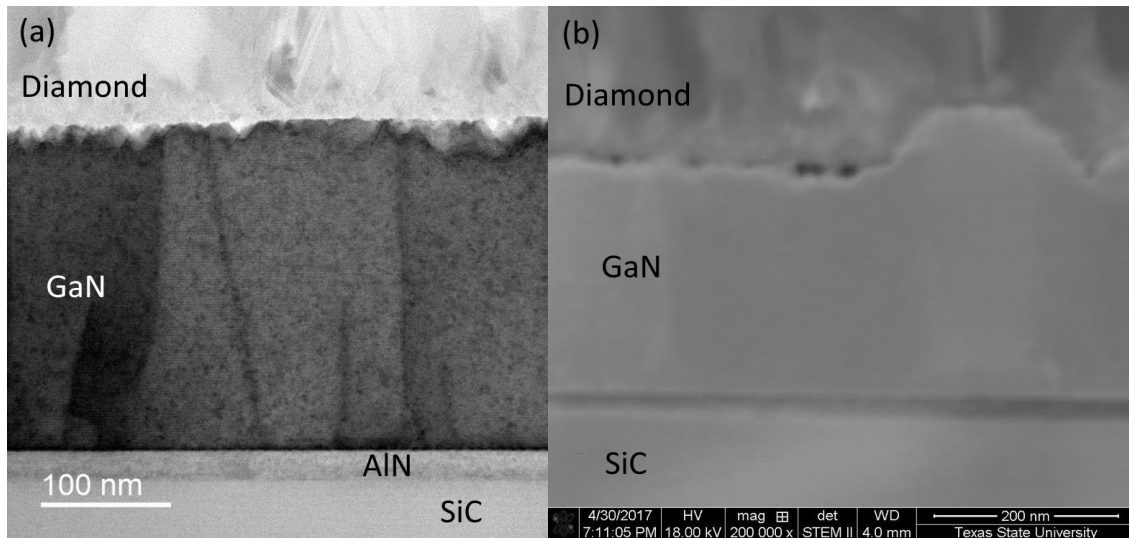


Figure 60. (a) Sample A TEM image showing good contact between the diamond and GaN with significant roughening of the interface. (b) SEM image of sample A showing small voids at the interface and demonstrating etching of the GaN where no AlN barrier is present.

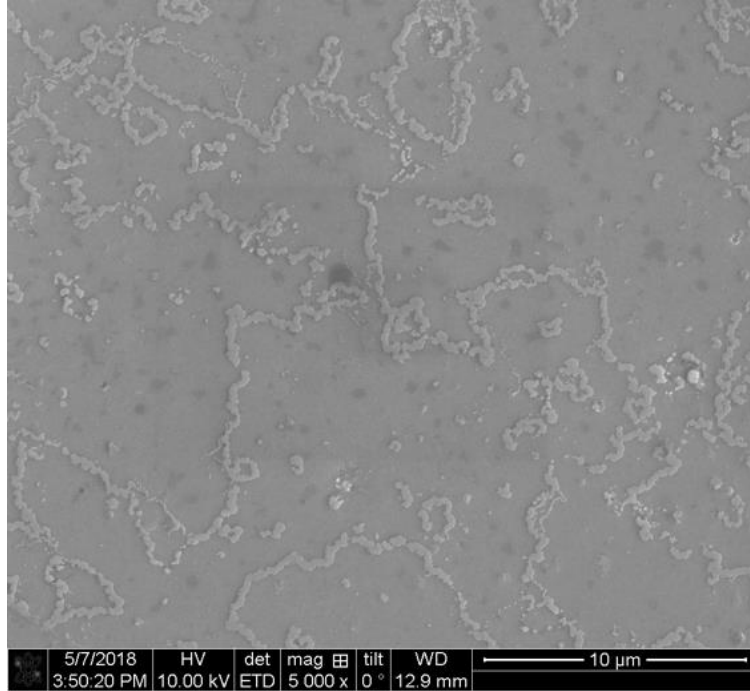


Figure 61. SEM image of sample A before the diamond deposition. The presence of mesa like structures (~40 nm height) are apparent before the diamond deposition (lighter areas are the mesas). This resulted in a non-uniform AlN deposition which allowed for roughening of the GaN during the diamond deposition

For sample S, a 3 nm wide amorphous region was identified using bright field STEM and can be seen in Figure 62. The diamond lattice planes can be clearly seen in the region above the amorphous layer. It is apparent that there is no etching of the GaN and the SiN interlayer provides a very clean transition between the GaN and diamond. The measured value of TBR for sample S was $9.5 \pm 3.8/-1.7 \text{ m}^2\text{K/GW}$. It is apparent that even with a relatively low thermal conductivity, SiN is the best choice of the three samples presented here for helping to facilitate the growth of diamond directly on GaN, and that due to the elevated temperatures and hydrogen rich environment, etching of the GaN during the growth must be considered.

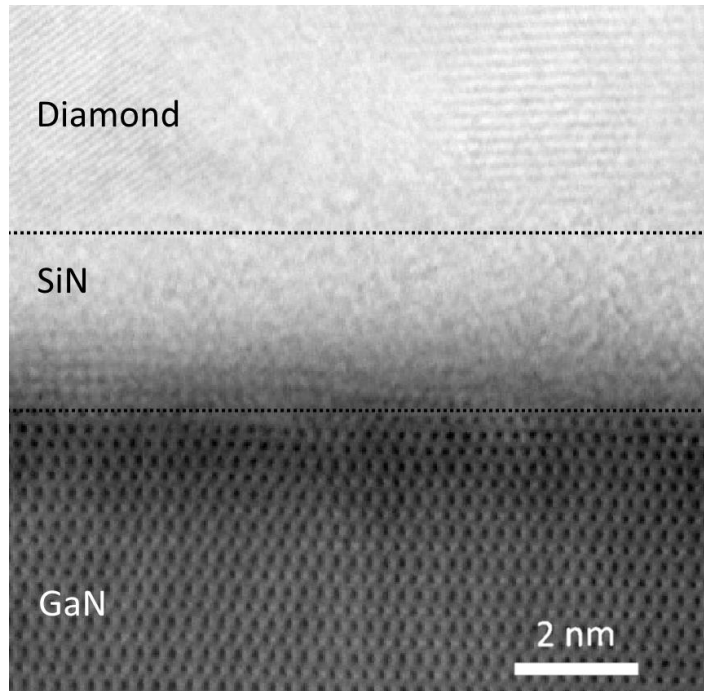


Figure 62. High resolution coherent bright field STEM image of sample S showing the diamond lattice planes and a ~3 nm of SiN acting as an etch barrier.

5.3.3 *Interface Characterization using Elemental Analysis*

The samples were analyzed using a JEOL ARM 200F microscope operating at 200 kV, and EELS was performed using a Gatan GIF Tridiem spectrometer. Imaging performed in a JEOL JEM-ARM300F Grand ARM TEM with a Gatan Quantum ER GIF was used to examine the distribution of the elements across the interface of samples A and S. It was observed in Figure 63 that in areas where AlN was present the etching of the GaN was reduced. The thickness of the AlN in Figure 63 is ~3.5 nm. This area is outlined in each of the images.

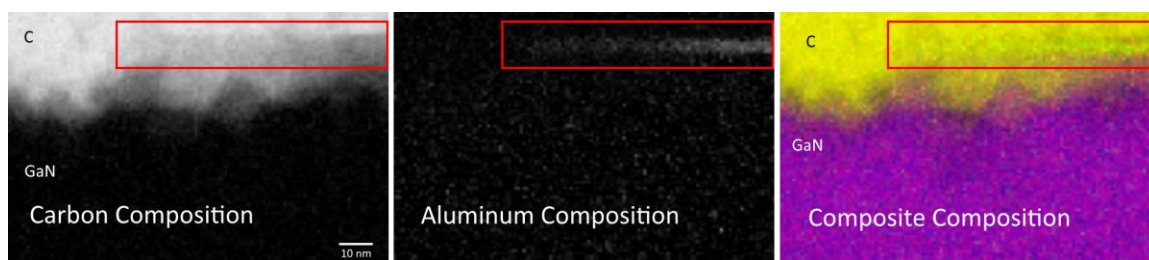


Figure 63. EELS composite imaging for Sample A (lighter areas indicate a larger present of the element). In the composite composition yellow is C, green is Al, and violet is GaN. It can clearly be seen that the AlN nitride layer (~ 3.5 nm) only occurs in select areas indicating a non-uniform deposition. Additionally, the AlN does act as an etch barrier where present.

An EELS spectrum image from the amorphous region of sample S is shown in Figure 64 and clearly indicates the uniformity of the SiN barrier layer. The composition mapping begins in the diamond and shows the changes moving across the interfacial layer into the GaN. There is a gradual decrease in the C composition over a range of about 4 nm, followed by the SiN region where the content of both Si and N increases in a nearly one-to-one ratio. The full width half max (FWHM), considering a Gaussian distribution, of the Si indicates a width of 3.2 nm. It is interesting that the carbon has the broadest distribution. This could be due to the formation of an amorphous layer near the interface. The data in Figure 64 demonstrates an ordered transition occurring at the diamond/SiN and SiN/GaN interfaces, with a small degree of intermixing at the SiN boundaries. Previous work to investigate how interfacial mixing and thin films can impact the TBR between two materials has been carried out by several groups. Hopkins *et al.* investigated Chromium/Silicon interfaces in which the deposition conditions were systematically adjusted to control the amount of interdiffusion between the Cr and Si [233]. They found that by altering the deposition conditions they could alter the size of the mixing layer, and in turn observe a change in the Cr/Si TBR. More recent work from Giri *et al.* has

demonstrated significant enhancement in interfacial thermal transport for a SiOC:H/SiC:H interface through the emergence of high frequency vibrational modes arising from atomic mass defects at the interface [234]. They were able to demonstrate a TBC approaching 1 GW/m²K for this material system.

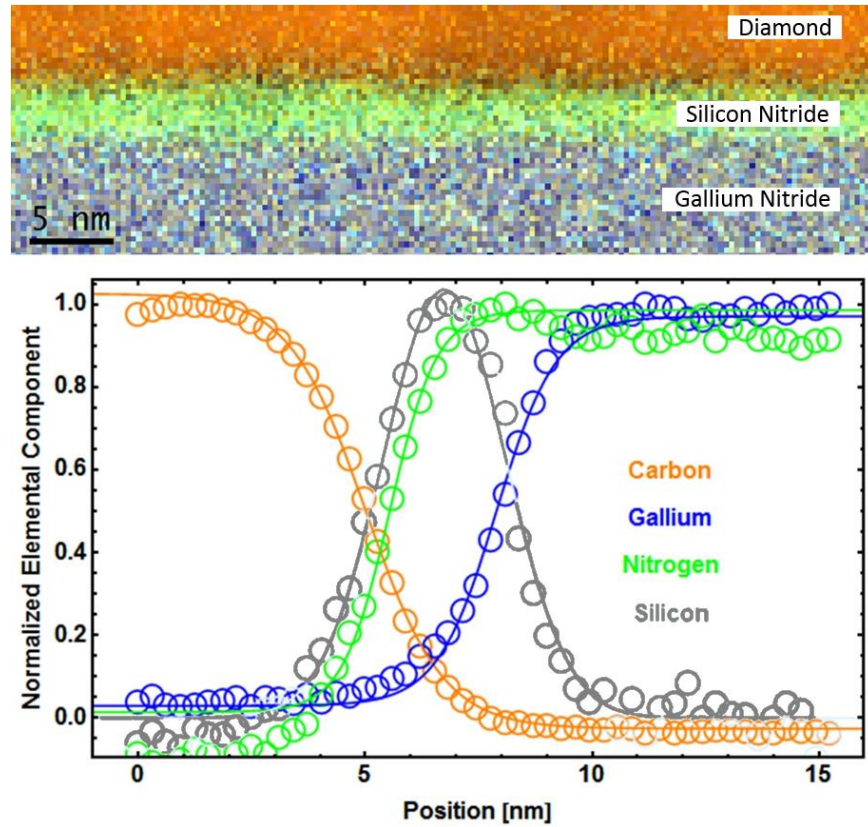


Figure 64. (Top) Composition mapping of a EELS map scan across the GaN/diamond interface. (Bottom) Averaged intensity along long direction in (Top) showing the elemental components of each section. The width of the Silicon section (FWHM of a Gaussian) is 3.2 nm. The difference between the Nitrogen and Gallium inflection points is about 2.4 nm. The σ in $\tanh[(x-\mu)/\sigma]$ is 1.7 nm for Carbon, 1.3 nm for Gallium, and 1.0 nm for Nitrogen. It is interesting that Carbon is the broadest, probably because of some amorphous layer at the surface. Gallium and Nitrogen are about equally sharp. Being $\frac{1}{4}$ of a degree of with a 80 nm thick sample produces an error of about 0.34 nm. This alone can be the source of the discrepancy.

While the main purpose of the AlN and SiN layer in these samples is to provide a dielectric coating and to protect the GaN from the hydrogen rich environment, it is also

worth noting that the inclusion of a thin film itself has been investigated as a means to enhance interfacial thermal transport. Several groups have explored the idea of using a thin interlayer to act as a vibrational bridge that will allow for coupling of phonon modes between two materials with significantly different phonon density of states [96, 103, 235]. Work from English *et al.* demonstrated through non-equilibrium MD simulations that by inserting an interfacial film material with intermediate vibrational modes it was possible to offset additional thermal resistance due to purely to diffusive transport in the added layer by a reduction in the effective TBR at both the new interfaces [103]. A recent study by Monachon *et al.* deposited amorphous Al₂O₃ interlayers, via ALD, ranging from 1.7 to 20 nm between both Al/Diamond and Al/Si [102]. They used TDTR to measure the effective Al/Diamond and Al/Si TBR. However, they did not observe any reduction in TBR with the inclusion of the Al₂O₃ interlayers.

Because the SiN and AlN interlayers used in this present work were both amorphous, it is hypothesized that the reduction in TBR comes mainly from the ordered transition rather than effects of coupling phonon modes. SiN thin film thermal conductivity has been measured to be as low as 0.34 W/m-K for a strained 50 nm thin film [236]. However, even with the low thermal conductivity of SiN, its ability to act as an etch barrier between the diamond growth environment and the GaN allows for a much smoother and ordered interface transition between the GaN and diamond, and the added resistance due to the SiN is less significant than the disorder displayed with both the sample G and A.

5.4 Conclusions

In conclusions, we have used TDTR to measure the thermal conductivity of a variety of CVD diamond samples. Bulk diamond samples were measured by two

laboratories that both used TDTR and it was found that there was good agreement between the Labs. These results were compared to flash diffusivity measurements that were provided by Lab 3, which was also the sample vendor. All the methods agreed well and it was found that highly boron doped samples had a significantly reduced thermal conductivity (674 W/m-K and 650 W/m-K) as compared to the higher quality bulk samples that had measured thermal conductivities of 1470 W/m-K, 1940 W/m-K, and 2200 W/m-K. One of the boron doped bulk samples was used to show the non-homogeneous thermal conductivity through systematically altering the measurement spot size and mapping within the diameter of a large spot. This work was further verified with high resolution mapping performed by Aditya *et al.*[210].

Evaluation of thin films was carried out on suspended diamond membranes grown on top of Si substrate. These measurements consisted of 1 μm films and showed that a significantly reduced cross-plane and in-plane thermal conductivity exists in these thin films due to grain boundary scattering disorder near the growth interface. A study of 2 μm films incorporated O_2 into the diamond growth to attempt to reduce sp^2 bonding. The thermal properties measurements indicated that the O_2 had a large impact on cross-plane thermal conductivity but not the in-plane thermal conductivity or the GaN/Si TBR. Additional thin films ranging from 5 μm to 13.9 μm were measured by GT and Lab 2. These films were found to have a thermal conductivity of 712 W/m-K for the 5 μm film and 1362 W/m-K for the 13.9 μm film. The trend indicated that the thermal conductivity was leveling off, indicating that thicker films would not see much more of an increase in thermal conductivity.

Finally, we used TDTR to measure the interfacial resistance of three different samples that contained diamond grown on directly onto a GaN layer. The samples consisted of differing interfacial conditions: sample G had no interfacial layer and the diamond was nucleated and grown directly on the GaN, sample A had a nominal 5 nm AlN layer deposited onto the GaN prior to diamond nucleation and growth, and sample S consisted of a nominal 5 nm SiN layer that was also deposited onto the GaN prior to the diamond growth. An extra sample that was also provided contained no diamond layer to help increase the accuracy of the TDTR method by first measuring the underlying material properties. Additional analysis using SEM, TEM, and EELS was performed to help understand and compliment the results of the TDTR experiments. It was discovered that for both samples A and G, etching of the GaN layer took place, resulting in a rough interface and in turn an increased TBR for these samples. Sample G demonstrated the highest TBR of $41.4 + 14.0/-12.3 \text{ m}^2\text{K/GW}$, and as it was discovered through the imaging techniques that the diamond had completely delaminated from the GaN for majority of the sample. Sample A showed the most significant amount of etching of the GaN during the growth, but still resulted in an interface that appeared to be in intimate contact with the remaining GaN even with significant roughening.

In addition, it was discovered through EELS analysis that sample A did not contain any Al between the GaN and the diamond in the etched GaN region. We attribute this to a non-uniform AlN layer on the GaN surface, resulting in smooth interfaces where the AlN is present, and the etching of the GaN where there is no AlN to act as an etch barrier. This sample's TBR was measured to be $18.2 + 1.5/-3.6 \text{ m}^2\text{K/GW}$. It is likely that with a uniform AlN layer, the TBR will be reduced further and may be equally as effective as the SiN

layer. Finally, sample S was found to have the lowest TBR of the three and demonstrated no etching or roughening of the interface. The measured value of TBR for sample S was $9.5 \pm 3.8/-1.7 \text{ m}^2\text{K/GW}$. It is apparent that even with a relatively low thermal conductivity, SiN is the best choice of the three samples presented here for helping to facilitate the growth of diamond directly on GaN, and that due to the elevated temperatures and hydrogen rich environment, etching of the GaN during the growth must be considered. It was also found through high resolution imaging and EELS analysis that a relatively smooth and ordered elemental transition takes place throughout the interlayer, thereby reducing disorder and enhancing phonon transport across the interface.

CHAPTER 6. THERMAL TRANSPORT IN VERTICAL GAN-ON-GAN PN DIODES

6.1 Overview and Approach

In order to look at the impact of passivation layers on the electrical/thermal performance for a set of GaN-on-GaN vertical diodes. Two sets of identical diodes are fabricated and only one is subject to a polyimide passivation. Electrical measurements are used to show the diode performance, which are followed by EL imaging that provides additional insight into the differences seen in the electrical performance. TDTR is used to evaluate the impact of p-type doping on the thermal conductivity of the GaN in the drift region of the diode. Transient thermal imaging allows for a full field view of the temperature distribution of the measured diode as well as provide information about the transient thermal time constant in the device. An FEM model is used to provide further insight into thermal device limitations when operating under a pulsed condition.

6.1.1 *Growth of GaN on Bulk GaN*

Unlike lateral devices that are grown on foreign substrates, GaN-on-GaN devices are able to be grown homoepitaxially directly on top of a GaN substrate. The growth method of the substrate will not significantly impact the ability to grow epitaxial GaN, however, the TDD present in the epitaxial layer will be directly impacted by the quality of the substrate. In this study we used a commercially available 420 μm thick 2" diameter HVPE n-type (Si) GaN substrate with a carrier concentration of $3 \times 10^{18} \text{ cm}^{-3}$ and a TDD of $3 \times 10^6 \text{ cm}^{-2}$. The epitaxial growth was carried out using MOCVD. During the growth

trimethylgallium (TMGa) and ammonia (NH₃) were used as precursors, and hydrogen (H₂) was the carrier gas, with monomethylsilane [SiH₃(CH₃)], and bis(cyclopentadienyl)magnesium (Cp₂Mg) used for the n-type and p-type dopants, respectively. The growth temperature was fixed at 1100 °C with a pressure of 1 atm. A growth time of approximately 5 hours resulted in a 15 µm n-type layer, a 500 nm p-type layer, and a 30 nm p⁺-type layer.

6.1.2 Sample Design

To create the PN junction, a 15 µm drift layer of n-type GaN was grown with a target carrier concentration of $7 \times 10^{15} \text{ cm}^{-3}$. This was followed by growth of a 500 nm p-type layer (Mg: $5 \times 10^{19} \text{ cm}^{-3}$) followed by a p⁺-type (Mg: $1.5 \times 10^{20} \text{ cm}^{-3}$) contact layer of 30 nm. Isolation of diode mesa structures were carried out with an inductively coupled plasma (ICP) etch using Cl₂ gas. Etching of the mesa structures was performed multiple times in order to achieve mesas with a height of 10 µm. The p-type GaN layer was then activated in a nitrogen rich atmosphere at 700°C for 5 minutes. Deposition of the anode contact was achieved with a 20 nm Ni adhesion layer followed by a 200 nm Au layer. Sintering and annealing of the metal was performed in an oxygen rich environment at 525°C for 5 minutes.

Two dies were created with the above process and a mask resulting in diodes with diameters of 130 µm, 330 µm, 520 µm, and 920 µm. One of the dies was subjected to additional 7 µm polyimide passivation by spin coating. The purpose of the passivation layer is to isolate the peripheral edge from electrical and chemical conditions in the environment; this allows for a reduction in reverse-current leakage, increases the breakdown voltage, and

raises the power dissipation rating. The two resulting sets of PN diodes are displayed in Figure 65. Details of the device layers are schematically shown in Figure 66.

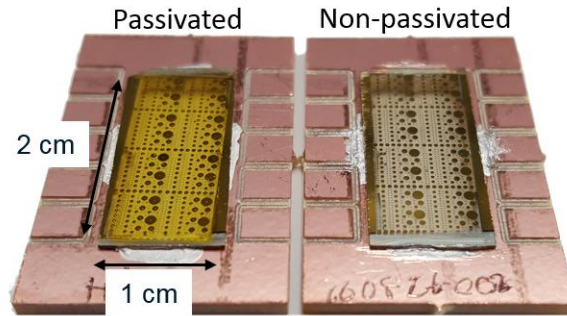


Figure 65. Completed PN diodes on direct bonded copper used to allow for measurement of the devices. The additional passivation is clearly seen in the left die by the yellow hue.

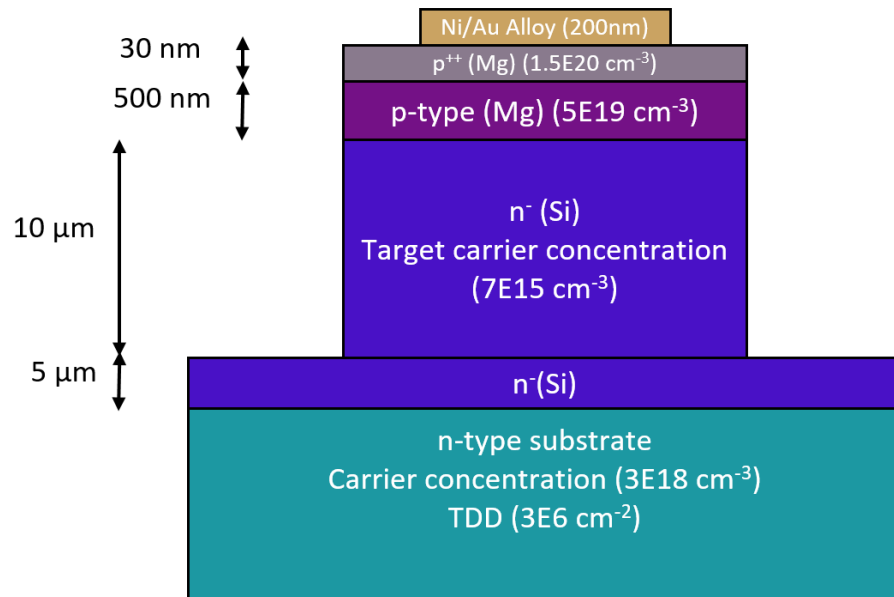


Figure 66. Schematic of devices structures without the passivation layer. All layers except the Au/Ni allow are GaN with the doping type and concentration indicated in the layer. The GaN substrate was 420 μm thick.

The quality of the diodes was assessed through Cathodoluminescence (CL) imaging in which the TDD was experimentally measured. The CL method uses an electron beam

to generate electron hole pairs in the GaN material, this causes a luminescence in the material that can be detected with a CCD. Locations in which dislocations are present the CL intensity drops and a well-defined “dark spot” is seen in the image. This technique has been compared to more invasive methods such as etch pit density and has shown excellent agreement in determination of TDD in GaN [237]. Figure 67 shows a $60\text{ }\mu\text{m} \times 80\text{ }\mu\text{m}$ region in which CL was performed on the epitaxial layer of our samples. Counting of the dislocations resulted in a TDD of $3.85 \times 10^6\text{ cm}^{-2}$. This is slightly higher than the TDD reported by the bulk GaN manufacturer which may indicate additional dislocations developing during the growth. Using this measured value we can then estimate how many dislocations are present on each of the diode mesas as indicated in Table 6.

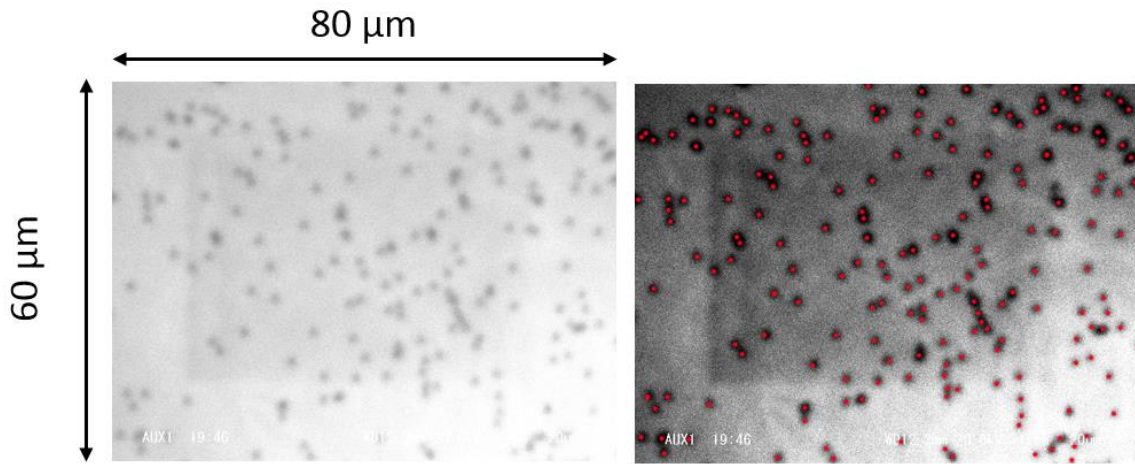


Figure 67. CL image of the epitaxial growth layer of GaN. Counting of the dislocations resulted in a TDD of $3.85 \times 10^6\text{ cm}^{-2}$.

Table 6. Correlation of TDD calculated from CL measurements with the diode diameters in order to estimate the total number of dislocations present in each diode.

Diode diameter [μm]	130	330	520	920
Approximate # of dislocations	302	2721	7559	30237

I-V characteristics of the devices were recorded and used to observe the specific ‘on-state’ resistance and breakdown voltage of each device. It was found that among the tested devices there was a significant difference in the breakdown voltage between the passivated and non-passivated devices. This was expected because of the dielectric effect of the passivation layer, however for these devices the difference in ‘on-state’ resistance is also shown to increase for the non-passivated devices for a voltage less than 10V. This information was then used to calculate a figure-of-merit for a GaN power diode based on Baliga’s Figure of Merit (BFOM) [8]. This parameter compares the breakdown voltage of a device with its specific on-resistance, and the results can be seen in Figure 68. It was found that the non-passivated devices demonstrated a lower BFOM because of the reduced breakdown voltage, while the larger diameter devices had a larger specific on resistance due to the large device area. In addition, many of the large diameter diodes experienced an early breakdown due to point defects in the GaN.

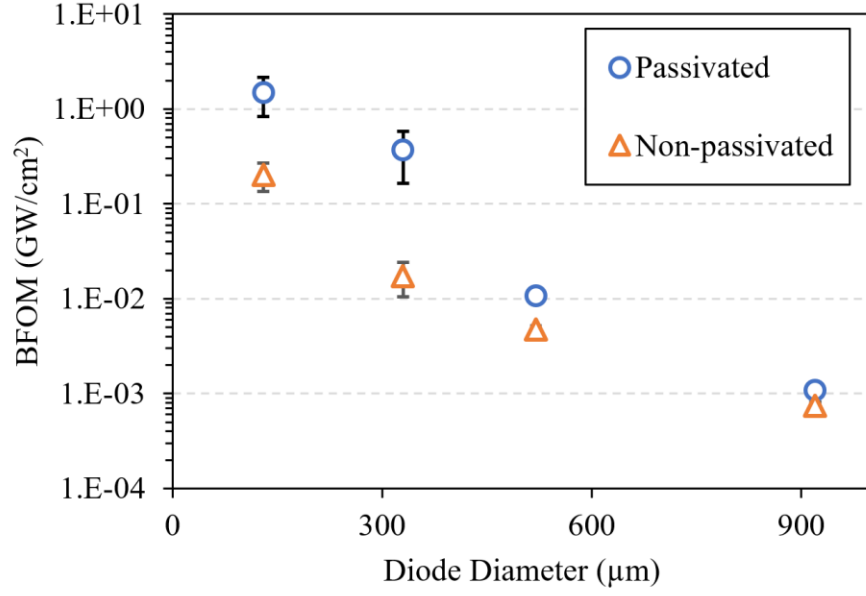


Figure 68. BFOM for power devices. Comparison between passivated and non-passivated devices with varying diameters.

Sections 6.2 and 6.3 will focus on the thermal aspects of the diodes by measuring the temperature rise in a 130 μm diameter diode through the use of transient thermoreflectance imaging and the measurement of thermal conductivity as a function of thermal penetration depth in the diode material using TDTR.

6.2 Transient Thermoreflectance Measurements

6.2.1 Theory and Experimental Setup

Similar to TDTR, transient thermoreflectance imaging (TTI) relies on the idea that reflectivity is a function of temperature. For a given temperature change the change in reflectivity can be related using a thermoreflectance coefficient. In mathematical form this is shown as:

$$\frac{\Delta R}{R} = \left(\frac{1}{R} \frac{\partial R}{\partial T} \right) \Delta T = C_{th} \Delta T \quad (40)$$

with C_{th} typically on the order of 10^{-2} - 10^5 K⁻¹, and can be either positive or negative. The thermorefectance coefficient strongly depends on the material, wavelength of illumination, and the angle of incidence. Accurate knowledge of the thermorefectance coefficient is paramount when using changes in reflectivity to estimate the surface temperature of a material.

For samples measured in this work a Microsanj NT220B was used. This system is capable of full field thermal imaging for a range of materials. Specific details of this system and its operation have been described in detail elsewhere [238, 239]. Operation of the system works by syncing a device pulse to that of an LED and CCD. First a duty cycle and power condition is applied to an electronic device, in this case the GaN PN diode, using an external pulse controller that is connected to the Microsanj system with an external trigger. For a given time before and after the prescribed duty cycle the CCD is open for exposure. During this same time the LED pulse is synced with that of the device. The temporal resolution of the transient measurement is determined by the LED pulse width and in this particular setup has a minimum resolution of 50 ns. The spatial resolution is directly related to the objective used. For a 100x objective used in this work we were able to achieve a resolution of 53.5 nm/pixel. In order to develop the full transient temperature profile, the LED pulse timing is delayed relative to the device pulse and the measurement of reflectivity is realized by a change in CCD intensity as compared to a reference. The CCD image is acquired over several seconds or even minutes allow for the accumulation of intensities that create a single image. In order to effectively take high quality images, it is

crucial that the focal plane remains constant. This is achieved through the use of a piezoelectric stage that accounts for thermal expansion during both the calibration and the measurement processes.

6.2.2 Thermorefectance Calibration

As mentioned, accurate knowledge of the thermorefectance coefficient is vital to provide as accurate temperature data as possible. Specific wavelengths have been shown to have very different thermorefectance coefficients that are also based on the material being probed. Figure 69 provides an example of how the thermorefectance coefficient for several metals will be impacted by the LED source wavelength [240].

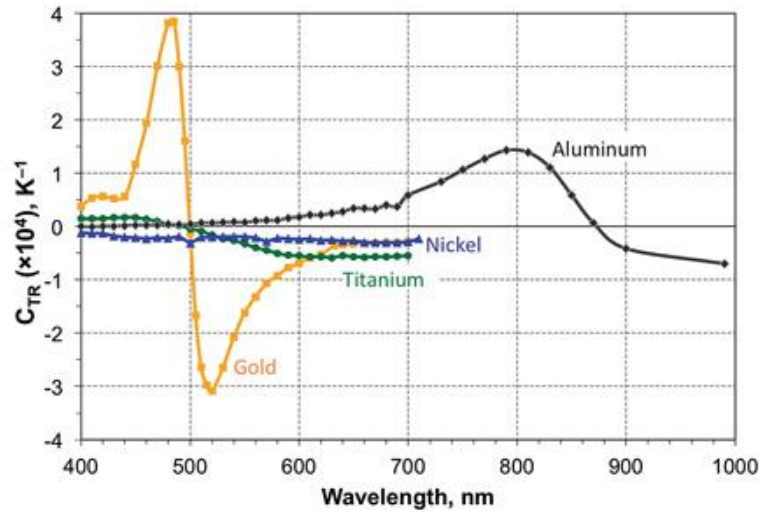


Figure 69. Thermorefectance coefficient for various metals as a function of wavelength [240].

For the samples used in this work, the thermorefectance calibration was performed at wavelengths of 470 nm and 530 nm. The diode samples were fixed to a copper apparatus

via a self-hardening silver epoxy and then securely mounted to the piezoelectric stage. In order to calibrate the thermoreflectance coefficient at these wavelengths the stage is heated to 100°C and then cooled back down to 20°C. Under the assumption that the thermoreflectance coefficient is linear, we obtain two data points in which to extract C_{th} . Figure 70 illustrates this concept for a positive thermoreflectance coefficient. The slope of the linear fit is C_{th} . There does exist thermal losses in the form of conduction resistance and convection from the assigned temperature stage and the actual temperature at the device. In order to mitigate this effect, we place a thermal couple as close to the measured device as possible and use the measured temperature for the calibration. Figure 71 shows temperature data measured during the calibration and it can be seen that we repeat the measurement several times to ensure a consistent value of C_{th} .

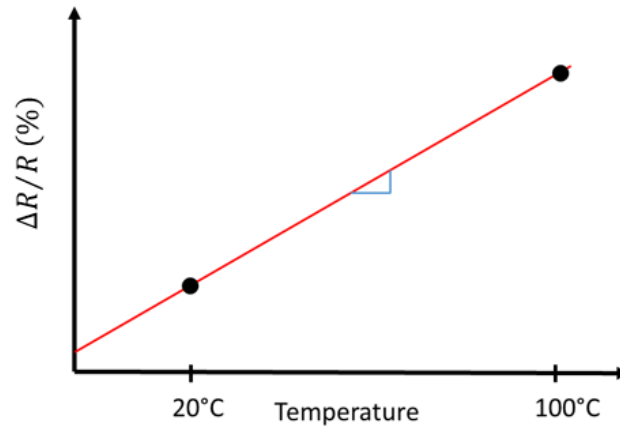


Figure 70. Illustration of method used to measure the thermoreflectance coefficient required for the measurement of temperature. The slope of the linear fit between the low and high temperature is C_{th} .

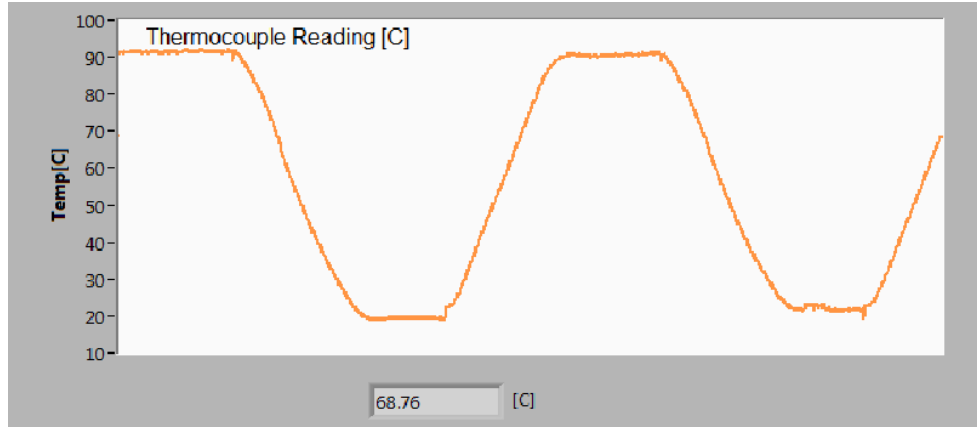


Figure 71. Measured temperature data from the coefficient calibration of the GaN PN diode. While the stage temperature is set to 100°C, the actual thermocouple reading near the device is closer to 90°C.

The measured location on the 130 μm diameter diode along with the measured coefficient at both wavelengths is shown in Figure 72 for each linear fit. From this data the thermorefectance coefficients were determined to be $2.53 \times 10^{-4} \text{ } ^\circ\text{C}^{-1}$ and $-2.08 \times 10^{-4} \text{ } ^\circ\text{C}^{-1}$ for the 470 nm and 530 nm LEDs respectively. These values are slightly different than what has been reported in literature [241]. This discrepancy reinforces the importance of independent measurements for the specific material systems under test. In our case, the Au contact had a 20 nm Ni adhesion layer deposited prior to the 200 nm Au and was then post annealed. In this case it would be expected that the thermorefectance coefficient would be similar to that of pure Au, with slight discrepancies as we see here.

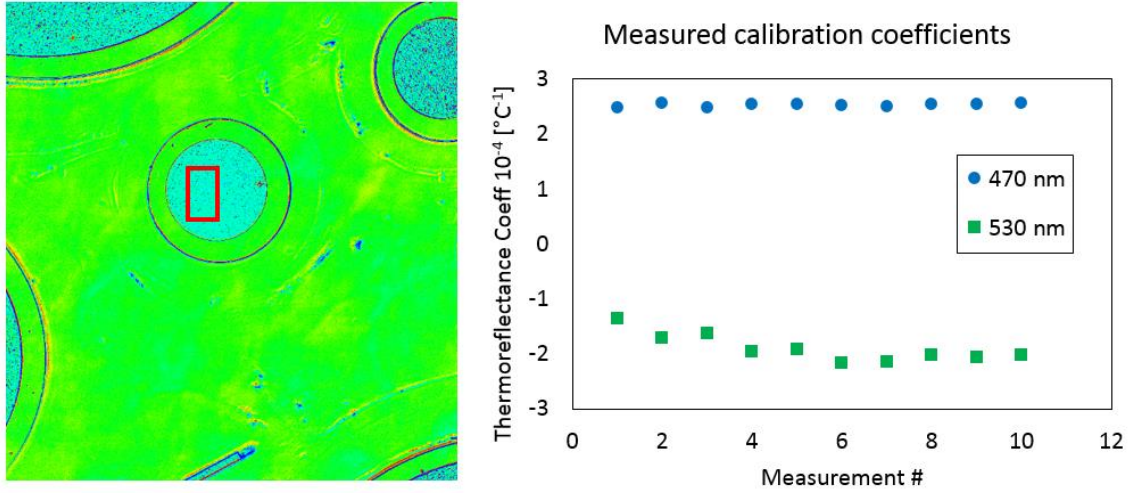


Figure 72. (Left) Thermoreflectance calibration image showing the measurement area of the 130 μm diameter diode. The thermoreflectance was only taken from the area with the Ni/Au metallization. (Right) Resulting thermoreflectance coefficients for both the 470 nm and 530 nm LED wavelengths at each measurement cycle.

6.2.3 Thermal Impacts of Device Passivation

Additional passivation may cause thermal concerns due to the low thermal conductivity of the passivation layer. Often thin layers of SiN are used as passivation and have been shown to have thermal conductivities as low as 3.2 W/m-K for a 2.3 μm film as measured by Mastrangelo *et al.* [242]. Here we used a polyimide film that was approximately 7 μm thick. Polyimide as a polymer has a significantly lower thermal conductivity of 0.12 W/m-K as reported by the material manufacturer. Both of these passivating materials have thermal conductivities that are several order of magnitudes lower than the GaN material active in the PN diode. In the case of diodes that heat is generated in the depletion region of the PN junction due to carrier recombination. Therefore, for the passivation to have any significant impact convection or radiation would have to play a significant role in heat removal from these systems. It is apparent that

conduction in the GaN is the dominate mode of heat removal from the source generation. Here we hypothesized that the contributions of convection and radiation to heat removal in these devices was negligible. This hypothesis was tested both through a finite element simulation and direct measurements of the passivated vs. non-passivated device through thermoreflectance imaging. The FEM simulations were performed in ANSYS and the device was modeled with quarter symmetry. Mesh refinement was performed in order to ensure an accurate representation of the heat transfer in the diode device. The modeled device with quarter symmetry and the resulting mesh are shown in Figure 73.

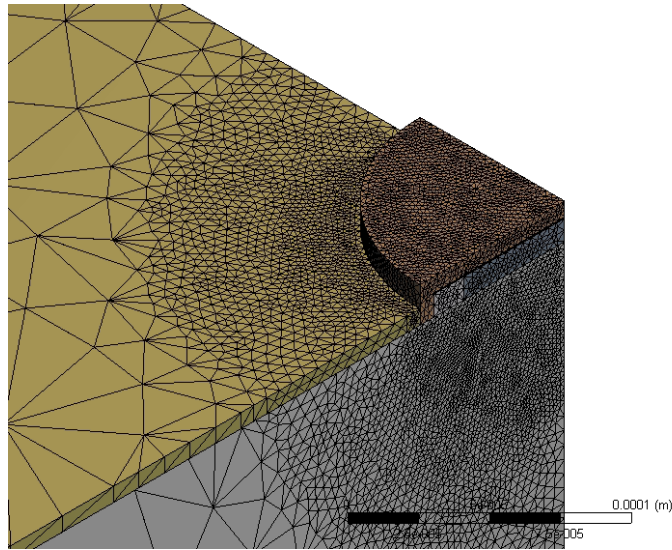


Figure 73. ANSYS model of GaN-on-GaN PN diode with polyimide passivation. The model uses quarter symmetry to reduce computational time and a fine mesh was implemented in and around the source of heat generation.

Thermal properties for the material were taken from literature and manufacturers reports. The simulation was performed as a steady-state heat transfer problem and included conduction, convection, and radiation. The thermal conductivities used were 0.12 W/m-K for the polyimide, 130 W/m-K for the p-type GaN layer, 160 W/m-K for the n-type GaN layer, and 200 W/m-K for the GaN substrate. These values are consistent with what has

been reported in literature [37, 180, 184] and have been experimentally verified using TDTR as will be discussed in Section 6.3. The quarter domain was 1.5 cm x 1.5 cm with insulated boundary conditions on the inside walls and a temperature boundary condition of 22 °C at the base of the substrate and the outside walls. The thickness of the layers was consistent with what was reported in Section 6.1.2. A convection heat transfer coefficient of 10 W/m² was applied on the surface of the model. Polyimide has been measured to have an emissivity of 0.6 [243] and GaN emissivity has been reported as high as 0.8 in literature [244]. For the purposes of this model, both the GaN and the polyimide coating were assumed to be blackbody emitters with an emissivity of 1, with radiation being applied on the surface of the model. The heat source was considered as internal heat generation in the volume that contained the n-type GaN present in the mesa structure. This material had a thickness of 10 µm. Heat generation was applied that resulted in 10 W of steady state joule heating in the device. It was first found that including the convection and radiation modes did not result in any temperature reduction as compared to considering the surface of the structure as perfectly insulated. This confirmed the idea that the only significant source of heat transfer in this device was a result of conduction. The maximum temperature in the simulation was 305.75 °C with the included polyimide film and 305.78 °C without the film, the difference of which is negligible and fully attributable to slight deviations in the model. Results of the thermal profiles obtained from the modeling can be seen in Figure 74.

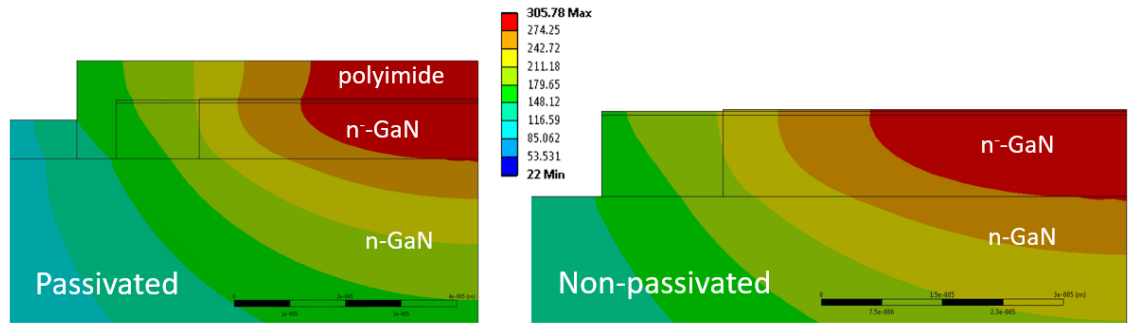


Figure 74. (Left) FEM model including additional polyimide film. (Right) FEM model with no polyimide. Both models resulted in a steady-state temperature of approx. 305 °C. It was found that because the main source of heat removal was through conduction. The polyimide film did not impact the overall temperature in the device as compared to a device with no passivation.

Additional verification of the impact of the passivation on the operating temperature of the devices was carried out using the thermoreflectance imaging technique previously described. As mentioned, the TTI method requires that the devices undergo a pulsed operation. Here the devices were operated at a 100 μ s pulse width with a total period of 400 μ s, resulting in a 25% duty cycle. Figure 75 shows the measured temperature rise for both the passivated and non-passivated devices as a function of peak pulse power. These powers were a result of voltage biases ranging from 9 V to 13 V. Most of the data demonstrates that there is no significant temperature difference between the two sets of devices, however, there does appear to be a slight deviation at higher voltage biases. It has not yet been determined if the discrepancy is due to the passivated device achieving a higher temperature or other experimental errors, as it does lie within the defined error bars.

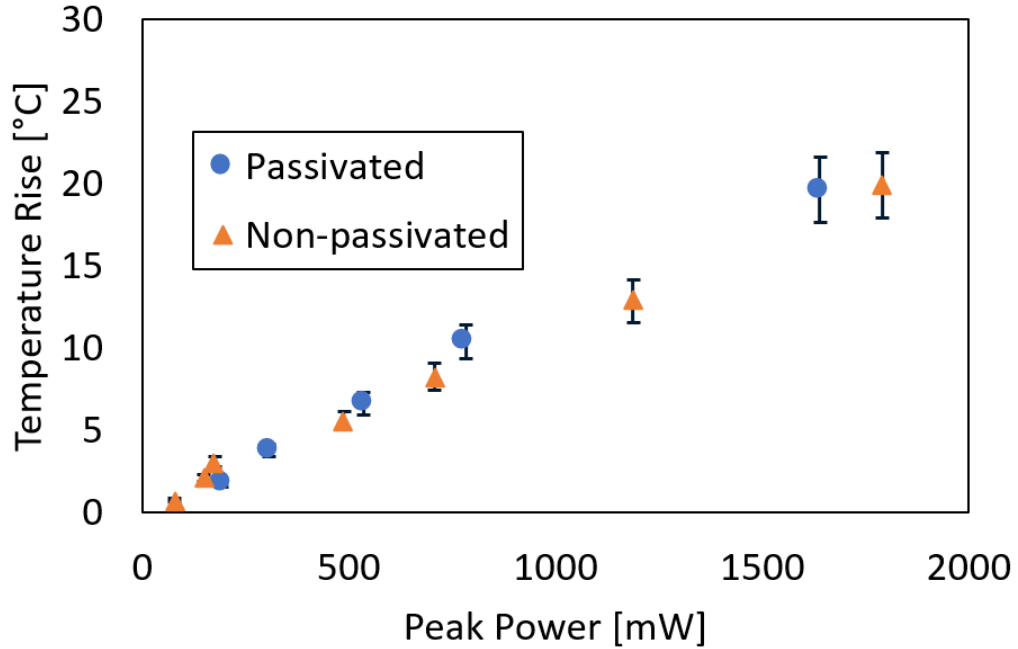


Figure 75. Temperature rise in both the passivated and non-passivated 130 μm diameter diodes vs. the peak pulse power as measured by TTI.

6.2.4 Heating under Large Forward Bias

Dependent on the diode application, it may be necessary for the diodes to handle relatively large currents during forward operation. The impact of passivation and subsequent heating was explored in this work. It was first shown through IV testing and electroluminescence (EL) imaging that non-passivated diodes were actually able to carry more current than the passivated diodes in this work at voltages greater than 10 V. This can be seen in Figure 76 as the applied voltage begins to surpass 10 V, the non-passivated devices overtake the passivated devices in terms of the current density maintained in the device. In order to explain this discrepancy, EL imaging was used to observe the areas of recombination in the diodes. The imaging was carried out at a voltage of 2.5 V where the voltage was just high enough to overcome the built-in potential barrier and allow for carrier

recombination to begin. As shown in Figure 77, the non-passivated devices were found to have significant carrier recombination at the surface of the mesa structure. This is due to the increase in surface states that would normally be contained by passivation of the electric field. However, with no passivation, these surface states are free to act as areas of surface recombination and therefore allow the non-passivated diodes to carry more current under a large forward voltage bias. It can clearly be seen that when the device is fully passivated there is no luminescence or recombination occurring at the mesa edge, where-as in the case with no passivation, surface recombination is apparent.

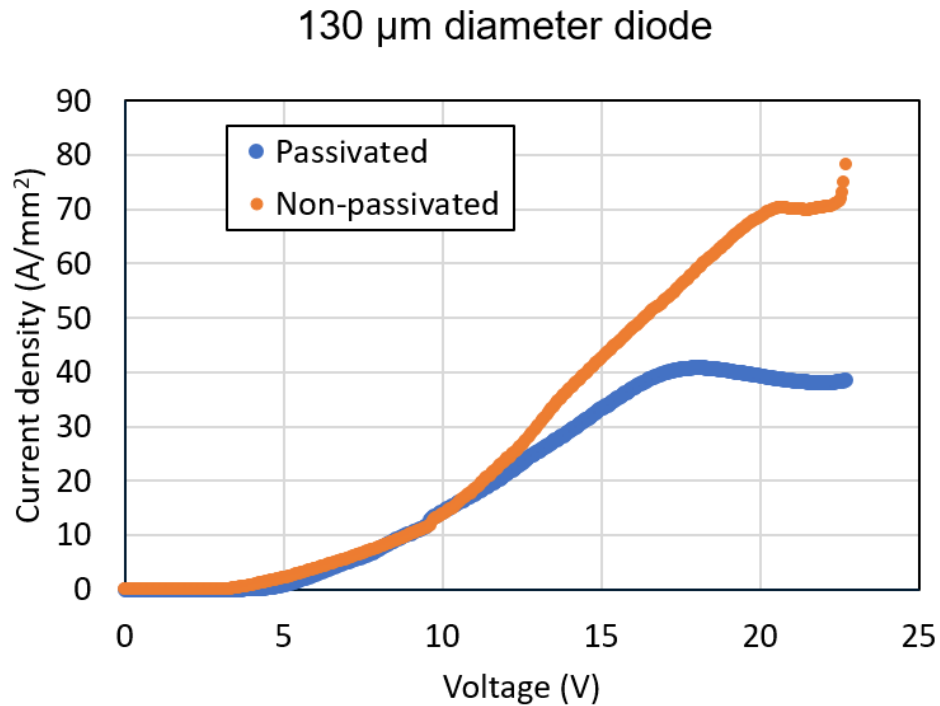


Figure 76. High voltage I-V characteristics for a 130 μm passivated and non-passivated diode.

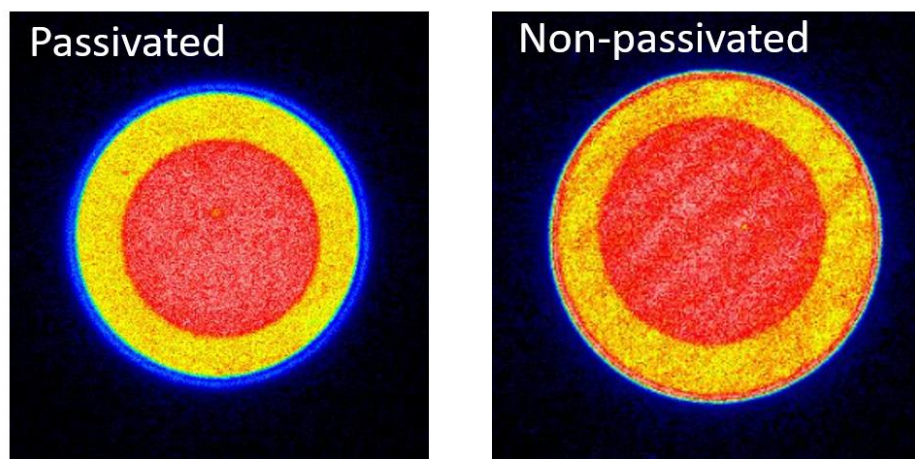


Figure 77. (Left) Passivated diode as measured by EL. (Right) Non-passivated diode EL measurement. It is clearly seen that when the device is passivated surface recombination effects are not present as they are in the non-passivated device.

Closer observation of the phenomenon in Figure 77 can be seen by looking at the cross-section of a diode. The diodes used in this work were cross-section using ion-beam milling in order to facilitate future work in which we will measure the temperature distribution through the cross-section of the diode. However, from the cross-sectioning, we were able to clearly see the impact of a non-conformal passivation. Figure 78 shows a top view optical image and an EL image of a passivated device that appeared to have a non-conformal coating. This is further confirmed in Figure by looking at a device cross-section.

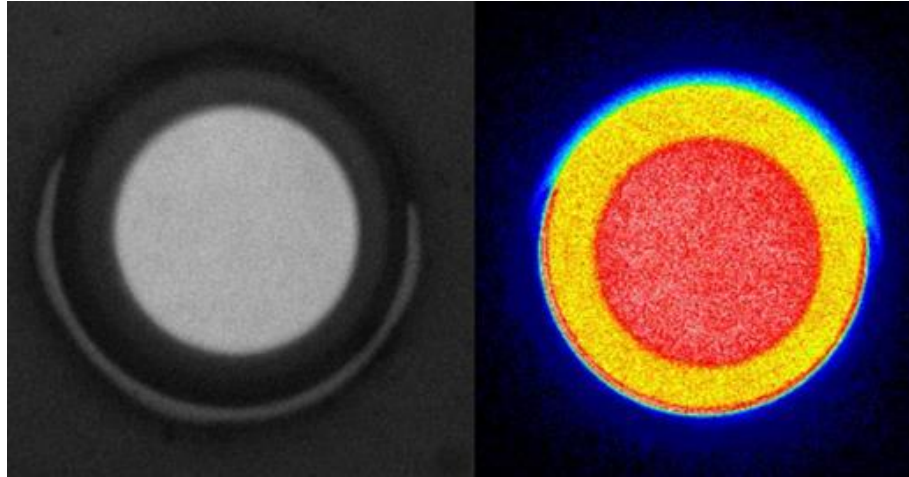


Figure 78. (Left) Optical image of a passivated device showing the non-conformal coating. (Right) Corresponding EL image that indicates additional surface recombination occurring at the mesa edge where passivation is not present.

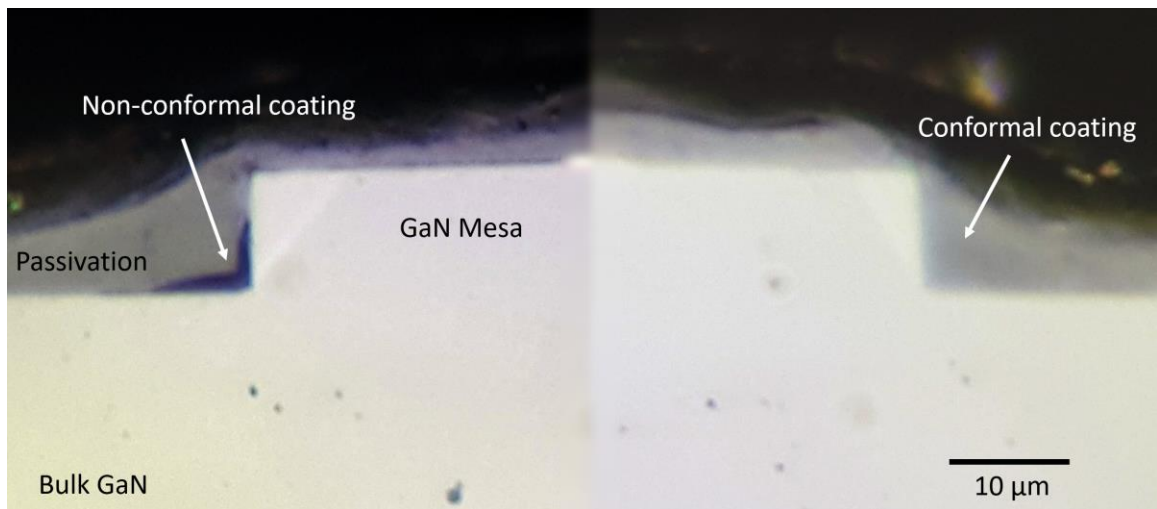


Figure 79. Optical image of device cross-section that clearly shows a non-conformal passivation coating on some of the mesa edges. This impacts the device performance by allowing surface recombination in these air gaps.

Figure 80 shows how a non-passivated 130 μm device increases in operational temperature as the voltage is increased. The power dissipated is the peak power of the individual 100 μs pulse, and the temperature is acquired at the end of the pulse. Forward voltages were increased from 10 to 19 V.

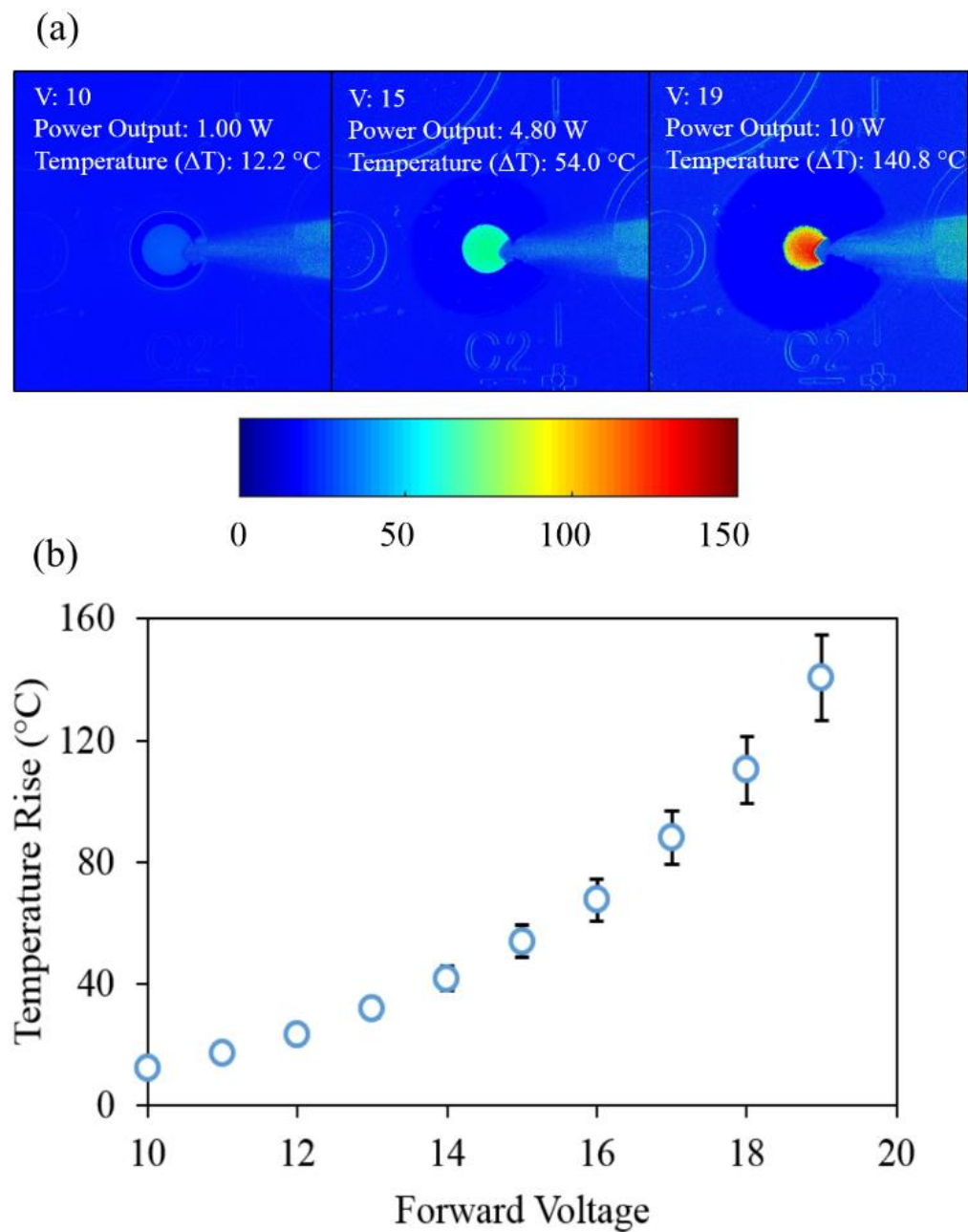


Figure 80. (a) Thermoreflectance images obtained during a large forward bias condition for a 130 μm non-passivated device. (b) Temperature rise for the same device at each of the tested forward voltages.

6.3 Non-homogeneous Thermal Conductivity

6.3.1 Impacts of p and n-type Doping on GaN Thermal Conductivity

The thermal conductivity of the GaN used to fabricate the diodes was evaluated using the TDTR method. For this evaluation the original 2” growth wafer was analyzed before the p-GaN activation. When using a pulsed heating technique, it is desirable to understand how the thermal penetration depth affects the measurement. In TDTR the thermal penetration depth is defined as [122]:

$$\alpha = \sqrt{\frac{\kappa}{C_v \pi f}} \quad (41)$$

where α is the thermal penetration depth (m), κ is the thermal conductivity (W/m-K), C_v is the volumetric heat capacity (J/m³K), and f is the frequency (Hz). This estimates the depth of the thermal wave and is indicative of how much of the material is sampled using a specific frequency with TDTR. For our experiments, we changed the modulation frequency of the pump beam in order to sample different depths of the material. Measurements were performed on both the top side with the p⁺ GaN layers as well as the backside that only contained the original 2” GaN substrate wafer. It was hypothesized that as the thermal penetration depth is decreased the topside of the wafer would experience a reduction in thermal conductivity through enhanced defect scattering in the p-GaN layers, and that the backside of the wafer would maintain a relatively consistent thermal conductivity regardless of the modulation frequency.

Figure 81 shows a schematic of the material system measured with blue and red arrows that coordinate with the measured thermal conductivity values. Figure 81 also shows an SEM image of the sidewall of a 130 μm diameter diode that was fabricated in this work. It is clear to see that near the surface of the mesa there exists significantly more disorder in the GaN material where the heavy p-type doping was present. Figure 82 shows the relationship between the thermal penetration depth, and the measured thermal conductivity of the GaN wafer. There is a reduced thermal conductivity even at larger thermal penetration depths for the topside of the wafer when compared to the backside, but there appears to be a steady decline in the thermal conductivity value as the thermal penetration depth is decreased on the topside. This effect is not as significant on the backside bulk substrate wafer. It does however show a small reduction at higher frequencies, most likely due to the mean free path dependence of phonons in GaN being comparable to the defect scattering length. The reduction in thermal conductivity from 162 W/m-K to 113 W/m-K on the topside of the GaN shows the effect of disorder and defect scattering that needs to be accounted for when modeling devices.

The thermal conductivity actually decreases with the enhanced p-doping creating a non-homogeneous thermal conductivity distribution through the diode device. Similar results have been shown by Beechem *et al.* [180] with large levels of Mg doping. Additionally, it has been shown that n-type doping with Si does not lead to significant reduction in thermal conductivity as compared to an equivalent p-doping concentration of Mg [180]. These results may help device designers better mitigate thermal issues by creating more accurate thermal models as the relationship between required doping and

thermal properties becomes more apparent. This could include altering specific growth recipes to attempt growth of doped layers with less disorder, or reduced thickness.

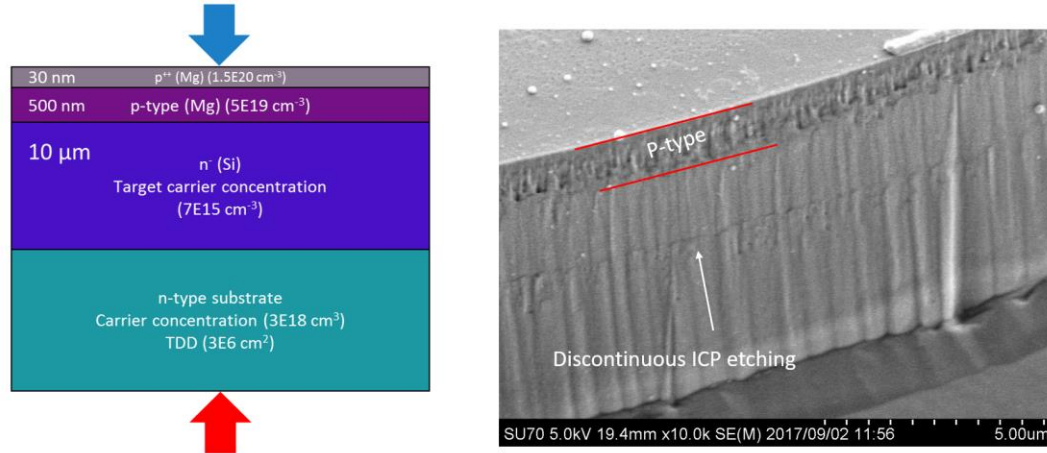


Figure 81. (Left) Schematic of the measured wafer demonstrating the different levels and types of doping in the epitaxial GaN layer. The color-coded arrows correlate with Figure 82 and demonstrate where the thermal conductivity measurements were performed. (Right) SEM image of the mesa sidewall for a 130 μm diameter diode. It appears that significant disorder exists near the top of the mesa where heavy p-type doping is present.

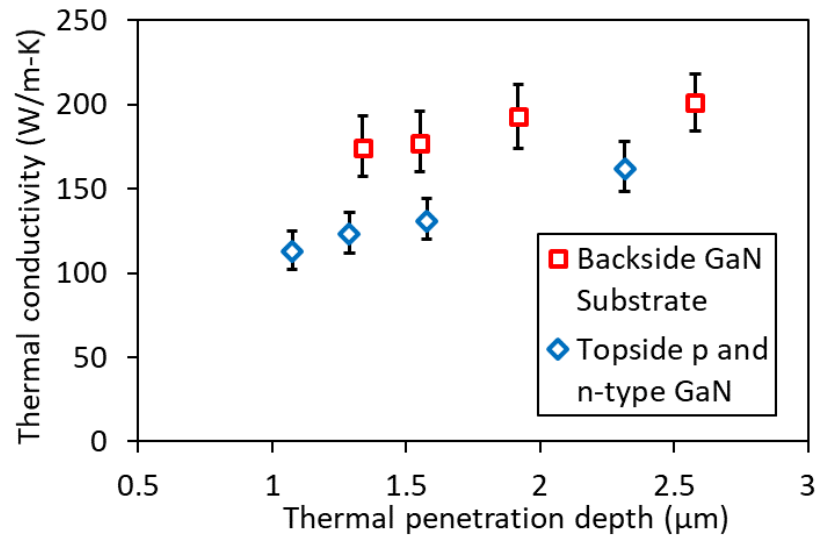


Figure 82. Thermal conductivity as measured by TDTR from both the backside GaN substrate and the topside of the wafer that was used to fabricate the PN diodes. A significant reduction in thermal conductivity is seen on the topside due to the high levels of p-type doping.

6.3.2 Impacts on Transient Device Operation

In almost all power electronic applications GaN devices will be operated in a pulsed mode or could be subject to a different power dissipation waveform that results in a time-dependent heating event in the diode. In order to increase the device reliability and lifetime, it is important to have a detailed understanding of the transient thermal behavior of the device. While there have been many cases of transient thermal modeling of GaN HEMTs in the literature using FEM models [245-247] and more recently analytical solutions [248], there still exists a lack of accurate modeling and experimental measurements of vertical GaN-on-GaN PN diodes. GaN based LEDs developed on sapphire substrates have been modeled under transient operation [249] however, these devices operate under markedly different conditions than a power diode. More recent work from Pavlidis *et al.* have looked at the transient thermal characteristics of both vertical and quasi-vertical GaN PiN diodes using both Raman thermography and TTI [26]. Their devices consisted on a 6 μm drift region and details of an additional buffer layer as well as mesa diameter were not revealed. Thus, a direct comparison to this work cannot be made, they did demonstrate that their GaN PiN diodes experienced a significantly reduced operating temperature and thermal time constant as compared to that of the quasi-vertical diode build on sapphire. Additionally, they showed that multiple time constants were necessary in order to accurately model the thermal characteristics of the temperature decay profile in their devices.

In this work, we subjected one of the 130 μm diameter devices to a pulsed form operation. The details of the pulsed operation were briefly discussed in the previous section, however, for clarity we will reiterate them here. The device tested was subjected

to a 100 μs pulse with a 12 V forward bias over a 400 μs period in order to result in a 25% duty cycle. This resulted in a peak power dissipation of 1.6 W. The details of the pulsed condition can be seen in Figure 83.

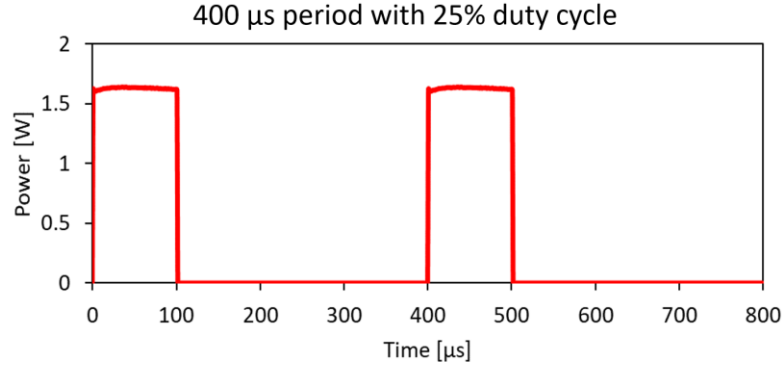


Figure 83. Pulsed conditions for a 130 μm diameter diode used in the transient thermal analysis. A 12 V forward bias was applied, resulting in a peak power dissipation of 1.6 W.

Measurements of the temperature rise were taken from the center of the diode anode metal and were consistent with what was reported in Figure 80. It was found that after 100 μs the device reach a near steady-state condition with a temperature rise of approximately 17.5 $^{\circ}\text{C}$. The transient thermal acquisition was carried out over 145 μs . This was not enough time for the device to fully dissipate all the heat and return to its original thermal state, although this was just the window for data acquisition, the actual device had 300 μs after the pulse in which to dissipate all the thermal energy. Modeling of the thermal time constants was considered with the following equation:

$$\Delta T = T_{\infty} \left[\sum_{m=1}^M 1 - C_m \exp\left(-\frac{t}{\tau_m}\right) \right] \quad (42)$$

where, T_{∞} is the steady-state temperature rise, C_m is a weighting parameter, and τ_m represents the thermal time constants. Figure 84 shows the measured data and its fit to equation 42 considering only a single time constant and two time constants.

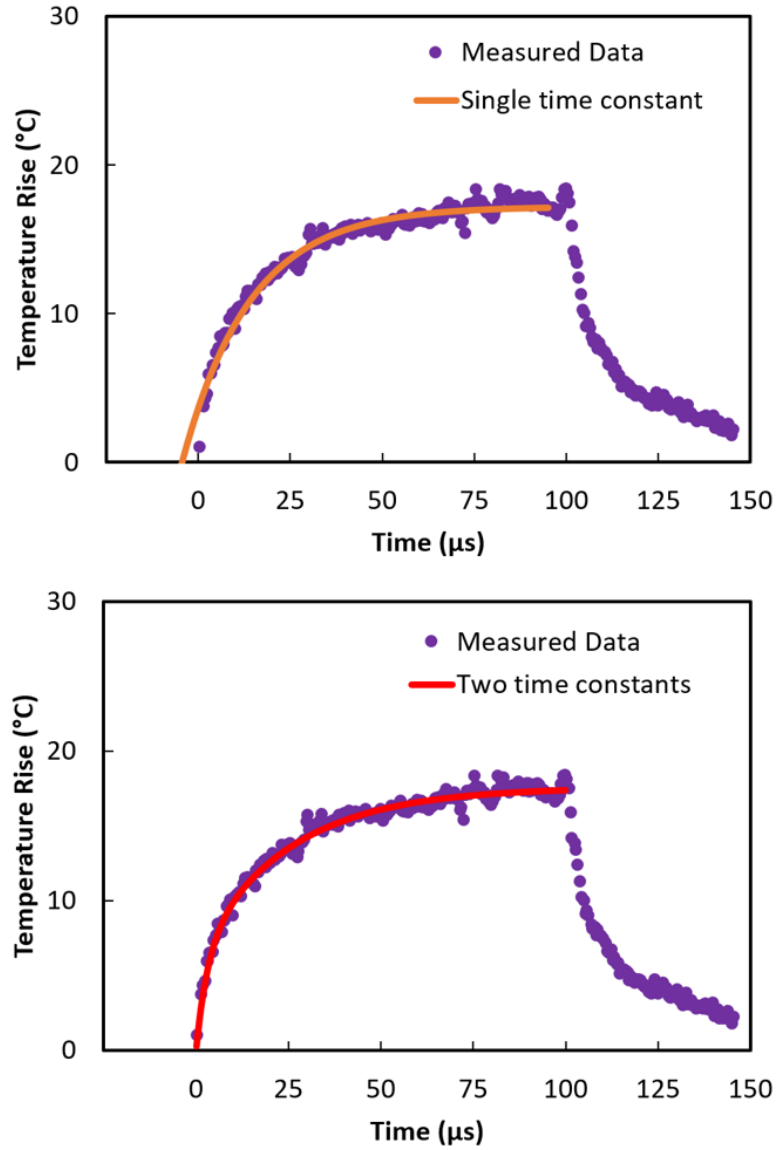


Figure 84. (Top) Measured data in TTI experiment with the temperature rise fit to equation 42 using only a single time constant. (Bottom) The measured data fit to equation 42 using two time constants.

In the single time constant case, fitting the data to equation 11 resulted in a steady-state temperature rise, T_{∞} , of 17.3 °C and a thermal time constant, τ , of 18.8 μ s. While the steady-state temperature is very close to the measured value, it can be seen from the data that at very early times the model does not accurately match the experimental data. However, if we allow for a second thermal time constant, we can see in Figure 84 that the model now accurately depicts the measured data. Here the steady-state temperature rise, T_{∞} , was fit to be 17.8 °C with thermal time constants of $\tau_1 = 3.1 \mu$ s and $\tau_2 = 24.9 \mu$ s. Here it is important to realize that the need for multiple time constants stems directly from the non-homogeneous thermal conductivity in the GaN material. As discussed, the heavy p-type doping led to a significant reduction in thermal conductivity near the top of the mesa, this in turn created a scenario where during transient operation there is a more significant temperature rise in the first few microseconds. If the material contained uniform thermal properties, multiple thermal time constants would not be necessary to accurately model the transient device behavior.

Finally, in order to better understand the appropriate duty cycle and how long thermal dissipation takes in this device, an FEM model was created based upon the thermal properties measured by TDTR and the device architecture. Similar to the model outlined in Section 6.2.3, quarter symmetry was used and the GaN thermal conductivity was varied as a linear function of distance based on the data in Figure 82. This resulted in the following equation used to represent thermal conductivity as a function of distance:

$$\kappa(x) = 38.97x + 71.29 \quad (43)$$

where x is the distance, in μm , from the top of the diode mesa moving downward into the material and k is the thermal conductivity (W/m-K) of the GaN material. Here it should be noted that the maximum thermal conductivity in the n-type drift region was considered to be 160 W/m-K consistent with previous reporting [180]. The thermal conductivity of the GaN substrate was considered to be 200 W/m-K. Other parameters in the model were consistent with those presented Section 6.2.3. Because this was a transient model, the volumetric heat capacity of the materials had to be implemented as well. For GaN a volumetric heat capacity, $C_v = 2.64 \text{ MJ}/\text{m}^3\text{K}$ was used and the anode contact was considered to only consist of Au with a $C_v = 2.49 \text{ MJ}/\text{m}^3\text{K}$, and a thermal conductivity, $\kappa = 315 \text{ W}/\text{m-K}$. Using a power input that was directly measured in the experiments and is shown in Figure 83 a transient FEM model was shown to match well with the experimental data. Figure 85 shows the FEM results as compared to the measured data through the measured time. Because during the initial measured time window that device did not fully dissipate the heat and return to its original temperature, the FEM model was extended to account for the entirety of the duty cycle as shown in Figure 85.

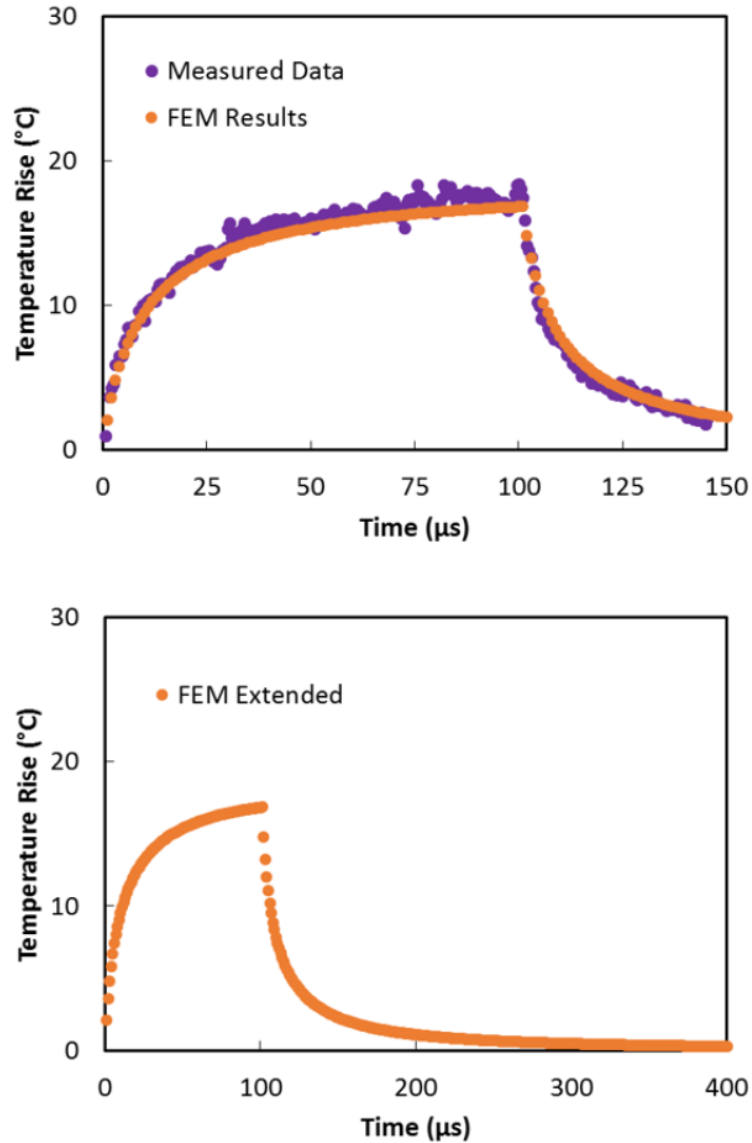


Figure 85. (Top) Measured temperature rise of the diode as compared to the FEM model for a time equivalent to the experimental data. (Bottom) FEM data extended out to 400 μ s in order to encompass the entirety of the duty cycle applied to the device.

After the full 400 μ s the maximum temperature in the model was found to be 0.27 °C. This indicates that a 25% duty cycle should be sufficient to fully dissipate the heat between pulses and avoid significant thermal accumulation in the device. Knowledge of appropriate thermal time constants and duty cycles are of critical concern when designing a GaN-on-GaN diode in order to ensure device reliability.

6.4 Conclusions

In conclusion, we have demonstrated the successful fabrication of vertical GaN-on-GaN PN diodes with structural, electrical, and thermal characterization of both passivated and non-passivated devices. It was observed that the polyimide passivation significantly increased the breakdown voltage and showed a lower on-resistance at forward voltages less than 10 V. Estimation of TDD in the MOVPE grown GaN was shown to be slightly larger than the manufacturer's GaN substrate using CL imaging. EL imaging was used to confirm the existence of an enhanced number of surface states without the use of passivation. This effect was further observed through a significantly higher current in non-passivated devices when applying a large forward bias. A comparison of the passivated and non-passivated device with TTI showed no significant temperature increase in the device during operation due to the additional passivation. This was further confirmed with FEM modeling. It was also demonstrated that there is uniform device heating at large forward bias and using TDTR we have shown that there is a significant reduction in thermal conductivity at the p-GaN surface that is depth dependent, which attributes to an overall heterogeneity in the GaN thermal conductivity in the diode devices. Transient measurements of at 130 μm diameter diode subjected to a pulsed power condition further demonstrated the impact of a non-homogeneous thermal conductivity in the mesa layer. It was found that two thermal time constants were required in order to sufficiently fit the experimental data to a thermal rise time model. This was shown with TTI and further verified by matching an FEM model to the experimental data. The FEM model was extended out to account for the full 25% duty cycle operation and it was found that this was sufficient to avoid the impact of thermal accumulation in the devices studied in this work.

CHAPTER 7. SUMMARY AND CONCLUSIONS

7.1 Summary of Contributions

The potential of GaN based electronics in both RF and power applications remains to be fully realized. While the development of high power transistors and diodes continues to advance rapidly, it is becoming more apparent that Si based technologies are approaching or have reached the theoretical limit of the materials capabilities. In order to continue the exceptional path the digital age as set us on, significant advancements in wide band gap electronics based on GaN must be realized. While commercially available power devices and RF devices are currently available, they must be severely scaled back in terms of operational voltages and power in order to account or device reliability issues. The reliability issues stem from many sources, electrical, structural, and thermal, which are all interconnected. Although, the thermal aspect of device reliability has consistently been overlooked during the design phase. It is for this reason that myself and many others are working diligently to provide valuable insight to the device community on how GaN based electronics are thermally impacted at the most basic device level. This is especially true with the AlGaIn/GaN HEMT device in which the extremely localized heat flux leads to both structural and thermal issues that cause device and material degradation.

The purpose and contribution of this work was to provide the reader with a sufficient motivation on the current and potential uses of GaN based electronics through a summary of the current state of the technology. This was followed by a more in-depth discussion of GaN devices by looking specifically at the AlGaIn/GaN HEMT and a vertical GaN-on-GaN diode structure. Basic principles and operation of an AlGaIn/GaN HEMT

were discussed to provide the reader with sufficient background. An introduction to vertical GaN device architecture in both transistor and diode configurations was introduced followed by relevant applications for all the aforementioned device types. The significance of GaN as used in a power electronics is emphasized in this work. This ties in to the device reliability issues that are then presented by looking at the localized heat source in GaN HEMTs and the thermal and stress management issues that arise during the device operation. A major emphasis of this work stems from the fact that lateral GaN devices are constructed on non-native substrates and because of this must undergo heteroepitaxy in order to grow the GaN on the substrate. This is achieved by introducing interfacial layers that allow for device quality GaN layers. The thermal impact of the TBR between the substrate and the GaN layers is explained to the reader through a series analytical models.

In order to introduce the reader to concepts and terminology used throughout the thesis, a portion is dedicated to providing an understanding of basic phonon transport as it is currently understood, with specific sections that focus on the approximations and models that are used to understand and estimate how heat/phonons transport across interfaces.

The characterization methods used in this work are discussed in sufficient detail, with emphasis on the need for optical methods based on the non-intrusiveness of the techniques as well as the accuracy. Specifically, TDTR is described in detail with a basic mathematical derivation that should be sufficient to guide any graduate student in the right direction when attempting to build a TDTR system or solve the TDTR equations. Sensitivity and uncertainty analysis of the TDTR approach are subsequently described in detail.

A complete study of GaN-on-Si devices and materials was undertaken that observed the impacts of residual stress in the device layers, the thermal properties of the GaN, and the overall impact on temperature rise in a device. This was followed by an analysis of thermal transport in CVD diamond for GaN-on-diamond devices by looking at both bulk diamond substrates and thin films. A complete study of the impact of dielectric layers the TBR between GaN and diamond was presented. Finally, a study of thermal transport in vertical GaN-on-GaN PN diodes was undertaken by evaluating the impact of polyimide passivation on device characteristics and heating. Followed by measurements of the thermal properties of the GaN due to doping effects with TDTR and full field transient thermal imaging of the device as compared to a thermal and FEM model to provide insight into thermal time constants and proper duty cycle operation.

7.2 Notable Achievements

- Complete study of a GaN-on-Si HEMT device that ties together the thermal limitations in the material by measuring the thickness dependent GaN thermal conductivity. This study clearly demonstrated how the inclusion of a SL structure impacted interfacial heat transfer and performance in a device by exploring the trade-offs between an increased GaN/Si TBR with the inclusion of a SL as a means to the residual tensile stress in the GaN. A series of HEMT devices consisting of both SL buffer layers and a much simpler AlN/AlGaN buffer were evaluated and it was clearly shown that the size dependent GaN thermal conductivity played a role in reducing the overall operational temperature through enhanced thermal transport and heat spreading effects.

- In order to understand the role of dielectric layers in thermal transport across GaN/diamond interfaces we observed that TDTR is capable of measuring the anisotropic and inhomogeneous thermal conductivity of CVD diamond near the interface as well as the TBR of the interface between GaN/diamond and GaN/Si. It was found that SiN acted as an etch barrier between the GaN and harsh growth environment of diamond, which allowed for a smooth interface and transition between the GaN/diamond.
- Fabrication of two sets of vertical GaN-on-GaN PN diodes that consisted of one with a polyimide passivation layer and the other without resulted in a demonstration of the surface recombination that occurs with no passivation. TDTR was used to measure a significantly reduced thermal conductivity near the surface of the diode mesa as a result of the heavy p-type doping. This led to a non-homogeneous thermal conductivity throughout the thickness of the GaN diode. The non-homogeneity was then shown to result in the need for multiple time constants to correctly model the transient temperature rise in the device. This was shown using TTI and further verified by a thermal model that indicated a 25% duty cycle was sufficient to avoid thermal accumulation effects in the devices studied in this work.

7.3 Future Work

Understanding of the thermal impacts of wide band gap electronics will need to continue in order to advance the technology. The most pressing need to continue the work of this thesis comes from advancing the measurement and manufacturing capabilities. For instance, in the case of the GaN/diamond interface study it was shown that AlN layer was

non-uniformly deposited. In this work it was also shown that in the areas of AlN deposition the GaN was protected from etching in the harsh diamond environment. Theoretically AlN even as thin film should have a higher thermal conductivity than SiN, so it would make sense that the next step in that study would be to ensure a uniform AlN deposition, or even better perform an in-situ AlN growth atop the GaN before the diamond deposition. This may result in a GaN/diamond TBR that is reduced even further.

Regarding the diode work, there is still much to be done to fully understand how the reduced thermal properties near the anode contact impact the overall temperature throughout the mesa. A cross-sectional thermal analysis using TTI while the diode is under a forward bias would be a significant step in better understanding the temperature distribution in the device. This work is currently underway as we have worked with collaborators to use ion beam milling in order to cross-section the diodes used in this work. An image of the cross-section is shown in Figure 86

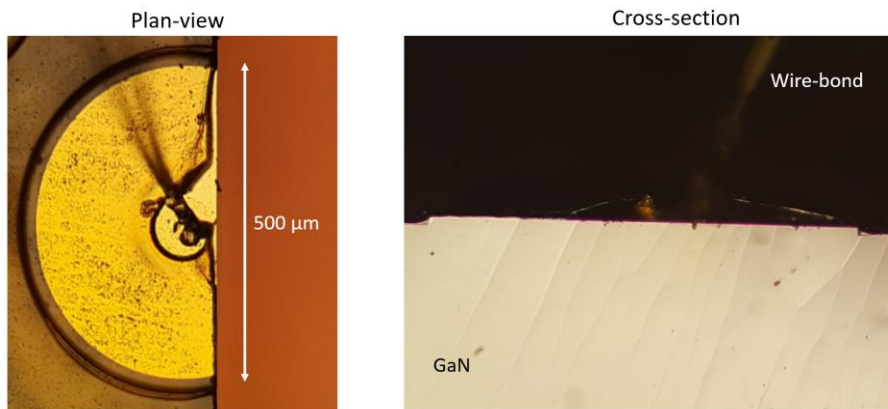


Figure 86. (Left) Plan-view image of a 530 μm diameter diode that has been cross-sectioned and wire-bonded. (Right) Cross-sectional optical image of the corresponding device that will be used to evaluate the temperature distribution through the diode thickness.

This type of measurement comes with many challenges, most significantly is the fact that the diodes luminesce, and the luminescence can interfere with the reflectance measurement captured by the CCD. The careful use of optical filters will be required to overcome this issue. It will also be critical that a proper smooth cross-section is acquired through the use of ion beam milling or other means. Thorough investigation of passivation methods including the use SiN will also be necessary to ensure the devices can be made and operated reliably. Many of the diode devices in this work experienced a non-conformal coating of the polyimide passivation at the mesa edge. This results in increased carrier recombination at the surface and provides an additional path for device breakdown.

GaN-on-Si technology is significant to power electronics because it is able to utilize some of the abandoned foundry equipment to create large area lateral GaN devices at a relatively reduced cost when compared to SiC substrates. A systematic study of how the SL periodicity impact thermal performance along with the correspond residual stress analysis would provide a great benefit in understanding the thermal and structural trade-offs that are incurred in a GaN-on-Si device.

Current methods such as TDTR and FDTR require the use of an additional transducer in order to absorb the laser energy and act as a uniform heat flux boundary condition in the model as well as allowing for proper reflectance off the sample onto the detector. Moving forward, it will be necessary to develop methods that do not require transducers to measure thermal properties. This is because of the large TBR that is present at the transducer/sample boundary. In order to increase the sensitivity of the underlying interfaces and gain a better understanding on how the TBR between epitaxial layers influences thermal transport this will be necessary. Removal of the transducer will require

a modification of the thermal model in order to account for optical penetration depth as well the use of high energy lasers that will absorb in the first 100 nm of material systems of interest. Much of this may require that systems be set up with multiple laser sources in order to allow for robust measurements over a range of materials.

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